Department of Electronics Engineering

Proposed Revised Curriculum Structure as per NEP2020

B. Tech. Electronics and VLSI Engineering

Sr. No.	Subject	Code	Schemes	Credits	Notional hours
Fifth Semester					
1	**Mandatory Core** Semiconductor IC Technology	VL301	3-0-2	04	85
2	**Mandatory Core** VLSI Design	VL303	3-0-2	04	85
3	**Elective – I**	VL3XX	3-0-2	04	85
4	**Elective – II**	VL3XX	3-0-0	03	55
5	**Institute Elective – I**	VL3XX	3-0-0	03	55
6	**Project Phase – I**	VL305	0-0-4	02	70
	Minimum Credit Requirement		**Total**	**20**	**435**
7	Minor / Honor (M/H#2)	EC3AA	3-0-2	4/**5**	70/85
8	Vocational Training/Professional Experience **(Optional) (Mandatory for Exit)**	ECV05/ ECP05	0-0-8	04	160 (20x8)
Sixth Semester					
1	**Mandatory Core** Analog VLSI Design	VL302	3-0-2	04	85
2	**Mandatory Core** VLSI System Design	VL304	3-0-2	04	85
3	**Elective – III**	VL3XX	3-0-2	04	85
4	**Elective – IV**	VL3XX	3-0-0	03	55
5	**Institute Elective – II**	VL3XX	3-0-0	03	55
6	**Project Phase – II**	VL306	0-0-4	02	70
7	**MOOC***	VL3XX	3-0-0	03	55
	Minimum Credit Requirement		**Total**	**23**	**490**
8	Minor / Honor (M/H#3)	EC3AA	3-0-2	4/**5**	70/85
9	Vocational Training / Professional Experience **(Optional) (Mandatory for Exit)**	ECV06/ ECP06	0-0-8	04	160 (20x8)

***NPTEL, SWAYAM and other Massive Open Online Courses (MOOC) approved by DAAC. As per 66th IAAC, Dated 20th March 2024, Resolution No. 66.34 and 61st Senate resolution No. 4, 25th April, 2024**

Subject Pool:

B. Tech. EC Elective -I (3-0-2)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Computer Architecture and Organization	VL321	3-0-2	4
2	Embedded Systems	VL323	3-0-2	4
3	Data Communication Networks	EC321	3-0-2	4

B. Tech. EVL Elective -II (3-0-0)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Semiconductor Device Modelling	VL341	3-0-0	3
2	Hardware Description Language	VL343	3-0-0	3

B. Tech. EVL Institute Elective – I (3-0-0)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Sensors and Transducers	EC361	3-0-0	3

B. Tech. EVL Elective -III (3-0-2)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Real-Time systems	VL322	3-0-2	4
2	VLSI Architecture for DSP	VL324	3-0-2	4

B. Tech. EVL Elective -IV (3-0-0)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Foundation of VLSI CAD	VL342	3-0-0	3
2	Memory Technology	VL344	3-0-0	3
3	Low Power VLSI Design	VL346	3-0-0	3
4	IoT and Applications	EC344	3-0-0	3

B. Tech. EVL Institute Elective – II (3-0-0)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Solar Photovoltaic Technology	VL362	3-0-0	3
2	Semiconductor Packaging	VL364	3-0-0	3

B.Tech. III (VL) Semester V SEMICONDUCTOR IC TECHNOLOGY VL301	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe and analyze material processing techniques and Pattern Transfer process
CO2	Explain, and compare the concept behind thin film deposition, and characterization techniques.
CO3	Describe, and compare metal contact formation, interconnect, bonding and packaging.
CO4	Demonstrates different fabrication, characterization, and metallization techniques.
CO5	Design basic semiconductor devices and their characterization.

2. Syllabus:

INTRODUCTION TO MICROELECTRONIC FABRICATION AND MATERIALS **(08 Hours)**

Semiconductor substrate: Crystal structure, Crystal defects, Crystal growth, Wafer fabrication and basic properties of Silicon Wafers, Wafer cleaning, and native oxide removal, Substrates beyond Silicon, Surface reactions, Dopants, Defects in epitaxial growth, Clean Room, and Safety requirements.

Diffusion, Thermal Oxidation, Ion implantation, Etching.

MASK FABRICATION AND ADVANCED LITHOGRAPHY TECHNIQUES **(06 Hours)**

Overview, Optical lithography, Photoresist, Mask Development, Patterning Strategies, Electron beam lithography process, EUV Lithography, X-ray lithography, and Other advanced lithography systems

THIN-FILM TECHNOLOGIES **(09 Hours)**

Physical Vapor Deposition: Evaporation Systems, Sputtering systems, and state-of-art Systems

Chemical Vapor Deposition: CVD system, Advanced CVD systems: LPCVD, UHCVD, AACVD, and advanced systems

Epitaxial Deposition: MOCVD, MBE, and CBE.

Solution-Based Deposition Techniques: Electrodeposition, Spin Casting, Printing, Layer-by-Layer Deposition, Colloidal Synthesis.

MEMS FABRICATION TECHNIQUES **(05 Hours)**

Silicon Pressure Sensors, Micro-Electro-Mechanical Systems, Micromachining Techniques, Isotropic Etching and Anisotropic Etching, Wafer Bonding, and LIGA Processes.

NANOSCALE DEVICE CHARACTERIZATION TECHNIQUES **(08 Hours)**

X-ray diffraction, X-ray photoelectron Spectroscopy, Spectroscopic Ellipsometry, Field Emission Scanning Electron Microscope, Transmission Electron Microscope, Atomic Force Microscope, Raman Spectroscopy, UV-Vis Measurement, Photo-Luminescence, Hall Measurement, Capacitance Voltage Measurement and Current-voltage measurement.

PROCESS INTEGRATION **(05 Hours)**

Contacts and metallization: Junction and oxide isolation, Si on insulator, Schottky and Ohmic contacts, Multilevel metallization.
CMOS technologies: Device behavior, Basic 3 µm technologies, Device scaling.

	Circuit Manufacturing: Yield, Particle control, Design of experiments, computer-integrated manufacturing.	
	INTERCONNECTS, BONDING, AND PACKAGING:	**(04 Hours)**
	Metallization, Silicides, CVD Tungsten Plug Process, Gold Wire Bonding and Other Bonding Technologies, Package Types, Assembly Techniques, Package Fabrication Technology, Package Design Considerations.	
	(Total Contact Hours: 45)	
3.	**List of Practical:**	
	1. Demonstration of processing steps involved in the cleaning of Silicon wafers. 2. Demonstration of microfabrication processes like oxidation, deposition, patterning, etc. 3. Demonstration of Thermal CVD deposition system. 4. Demonstration of DC/RF Sputtering system. 5. Demonstration of Thermal evaporation setup. 6. Electrical properties estimation of the thin film materials using Four Probe Hall Effect measurement setup. 7. Demonstration of Spin Coating and Hydrothermal Process for the material growth. 8. Current-Voltage characteristics measurement using semiconductor parameter analyser for different semiconductor devices. 9. Demonstration of UV-Visible absorption measurement. 10. Demonstration of Raman spectrometer measurement. 11. Simulation of microfabrication processes like oxidation, deposition, patterning, etc. using TCAD tool	
4.	**Books Recommended:**	
	1. Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication”, 2nd edition Oxford University Press, 2001. 2. S.M. Sze (Ed), “VLSI Technology”, 2nd edition McGraw Hill, 2017. 3. Hrundle, Evans, Wilson, “Encyclopedia of Material Characterization”, Elsevier, 1992 4. D. K. Schroder, “Semiconductor Material and Device Characterization”, Wiley Interscience, 2016 5. James Plummer, M. Deal and P.Griffin, “Silicon VLSI Technology”, Prentice Hall Electronics, 2003. 6. Plummer, Deal, Griffin, “Silicon VLSI Technology Fundamentals Practice and Modeling”, Pearson Education Limited, 2014. 7. Rao R. Tummala, “Fundamentals of Device and Systems Packaging Technologies and Applications”, McGraw-Hill Publications, Second Edition, 2019.	
5.	**Additional Resources:**	
	1. Relevant Journals and Conference publications.	

B.Tech. III (VL) Semester V VLSI DESIGN VL303	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe VLSI Design flow and circuit characterization for performance estimation.
CO2	Demonstrate dynamic Logic circuits.
CO3	Compare different semiconductor memories.
CO4	Evaluate the circuit performance using Logical efforts.
CO5	Design arithmetic building blocks (data-path) from the system's perspective along with the design of FSM (Control-path).

2. Syllabus:

INTRODUCTION OF VLSI DESIGN **(06 Hours)**

Historical Perspective, Design Hierarchy, Concepts of Regularity, Modularity and Locality, VLSI Design Styles, VLSI Design Flow, Semi-Custom- Full Custom IC Design Flow, Data Path, Control Path Programmable Logic Array, CMOS and Bipolar Transistor Gate Arrays and Their Limitations, Standard Cells, FPGA/CPLD Architecture.

DYNAMIC LOGIC CIRCUITS **(06 Hours)**

Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic and High Performance Dynamic CMOS Circuit, Dynamic Latches and Registers.

CIRCUIT CHARACTERIZATION FOR PERFORMANCE ESTIMATION **(08 Hours)**

Interconnect, Estimation of Interconnect Parasites, Delay Estimation, Logical Efforts and Transistor Sizing, Power Dissipation, Design Margin, Reliability.

SEMICONDUCTOR MEMORIES **(08 Hours)**

Type of Memories, design and analysis of ROM Cells, Static and Dynamic Read - Write Memories, Memory Peripheral Circuits, Power Dissipation in Memory, Flash Memory

DESIGN OF ARITHMETIC BUILDING BLOCKS **(12 Hours)**

Data Path Operations: Adders, Shifter, Multiplier, Power and Speed Trade-off in Data-path Structures, Control Path and FSM.

INPUT-OUTPUT CIRCUITS **(05 Hours)**

ESD Protection, Input Circuits, Output Circuits, Pad Drivers and Protection Circuit, On-Chip Clock Generation/Distribution, Latch-up and its Prevention.

(Total Contact Hours: 45)

3. List of Practical:

1. Design and simulate CMOS Inverter standard cell using CADENCE.
2. Layout and simulate CMOS Inverter standard cell using CADENCE.
3. Introduction to Verilog HDL and FPGA.
4. Implementation and Simulation of Logic Gate using Verilog HDL on FPGA
5. Design and Implementation of Half adder and Full Adder using Verilog HDL on FPGA.
6. Design and Implementation of Half subtractor and Full Subtractor using Verilog HDL on FPGA.
7. Design and Implementation of Ripple Carry Adder using Verilog HDL on FPGA.

	8. Design and Implementation of Multiplexer using Verilog HDL on FPGA. 9. Design and Implementation of Flip-Flops using Verilog HDL on FPGA. 10. Design and Implementation of Registers using Verilog HDL on FPGA. 11. Design and Implementation of Four Bit Up-Down Counter using Verilog HDL on FPGA. 12. Design and Implementation of Array Building Blocks.
4.	**<u>Books Recommended:</u>**
	1. Rabaey Jan M., Chandrakasan Anantha and Borivoje Nikolic, "Digital Integrated Circuits (Design Perspective)", 2nd Ed., Prentice Hall of India, 2016 (Reprint). 2. Kang and Leblebici,“CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, 4th Edition, 2019 3. Baker R. Jacob, Li H. W. & Boyce D. E.,“CMOS Circuit Design, Layout And Simulation”, Wiley, 4th Edition, 2009 4. Weste and Harris,“CMOS VLSI Design: A Circuits and Systems Perspective”, Pearson Education, 4th Edition, 2020 5. Pucknell and Eshraghian: “Basic VLSI Design”, Prentice Hall of India, 3rd Edition, 2003

B.Tech. III (VL) Semester V COMPUTER ARCHITECTURE AND ORGANIZATION VL321	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Identify the functional architecture of computing systems.
CO2	Estimate the performance of various classes of machines, memories, pipelined architectures etc.
CO3	Compare CPU implementations, I/O methods etc.
CO4	Analyze fast methods of ALU, FP, and Control unit implementations.
CO5	Implement an instruction encoding scheme for an ISA and Build large memories using small memories for better performance.

2. Syllabus:

DESIGN OF INSTRUCTION SET ARCHITECTURE (ISA) **(11 Hours)**

Various Addressing Modes and Designing of an Instruction Set, Concepts of Subroutine and Subroutine call and return, Introduction to CPU design, Instruction Interpretation and Execution, the instruction set of a modern RISC processor, including how constructs in high-level languages are realized, concept of pipeline

PROCESSING UNIT **(13 Hours)**

The representation of both fixed- and floating-point numbers, together with hardware algorithms for fixed-point arithmetic operations; Basic processor organization, ALU sub-system, Data path in a CPU, Instruction cycle, Organization of a control unit - Operations of a control unit, Hardwired control unit, Micro-programmed control unit.

MEMORY SUBSYSTEMS **(11 Hours)**

Memory Hierarchy; Cache memory design, Cache Mapping, Write and Replacement policy, Virtual Memory, A Real-World Example of Memory Management, DMA Controller, Overview of SRAM and DRAM Design; Memory bus between CPU and DDR3/DDR4 based SDRAM, Memory controller for DDR3/DDR4.

BUSES AND PROTOCOLS **(10 Hours)**

Introduction to Input/output Processing, Programmed Controlled I/O transfer, Interrupt Controlled I/O transfer, Introduction to serial and parallel Bus systems, Popular bus architecture standard such as IDE, SCSI, ATA, SATA, USB and IEEE 1394, Network component and protocols such as Ethernet and CAN.

PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY **(30 Hours)**

(Total Contact Time: 45 Hours + 30 Hours = 75 Hours)

3.	**List of Practical:**
	1. Implementation of Binary Adders 2. Implementation of Booth's Multiplier 3. Implementation of Wallace Tree Multiplier 4. Implementation of Division Unit 5. Implementation of Instruction Decoder 6. Implementation of Datapath with FSM 7. Implementation of Control Unit - Hardwired Control 8. Implementation of Control Unit - Microprogrammed Control 9. ALU Design using existing blocks 10. Implementation of Cache Memory Design – Direct Mapped 11. Implementation of Cache Memory Design – Associative Mapped 12. Overall CPU design
4.	**Books Recommended:**
	1. David. A. Patterson and John L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 5th Ed., Morgan-Kaufmann Publishers Inc. 2014 2. Linda Null and Julia Lobur, "The Essentials of Computer Organization and Architecture", 5th Ed., Jones & Bartlett Learning, 2018 3. Alan Clements, "Principles of Computer Hardware", 4th Ed., Oxford University Press, 2013 4. C. Hamacher et al., "Computer organization," 6th Ed., TMH, 2012
5.	**Reference Books:**
	1. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd Ed., McGraw-Hill, 2013 2. M. Morris Mano, "Digital Design", 6th Ed., Pearson Education, 2018

B.Tech. III (VL) Semester V EMBEDDED SYSTEMS VL323	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe ARM processor, its modes, exception handling, instruction pipelining and basic programming
CO2	Implement Assembly and C language programming for ARM Cortex-M.
CO3	Analyze 32-bit ARM microcontroller architecture, External Memory, Counters & Timers, Serial Data Input/Output and Interrupts. Design for interfacing Keys, LED/LCD Displays, ADC And DAC
CO4	Evaluate concepts of RTOS and its functionalities.
CO5	Design a typical cost-effective real-world embedded system with appropriate hardware components and software algorithms

2. Syllabus:

OVERVIEW OF EMBEDDED SYSTEMS **(06 Hours)**

Embedded Vs General computing system, Classification of Embedded systems, Major applications, Quality Attributes of Embedded Systems, Typical components, Embedded software development, Embedded OS, RISC Vs CISC Architectures

ARM CORTEX M3/M4 ARCHITECTURE **(10 Hours)**

Overview of ARM Cortex family, Operation modes and states, Registers, Special Registers, Floating point Registers, Application program status registers, Memory system and MPU, Exception and interrupts, System control block, OS support features

PROGRAMMING CORTEX M3/M4IN ASSEMBLY/C **(12 Hours)**

Assembly Instructions: Data Processing, SIMD and saturating, Multiply and MAC, Packing and unpacking, Floating point, Data conversion, Bit field processing, Compare and Test, Branching, Sleep mode, Memory barrier and other instructions, Assembly and Embedded C programming examples

PERIPHERAL INTERFACING **(08 Hours)**

Serial Communication interfacing such as USB, RS485, SPI, I2C, CAN and Ethernet, Motor control with PWM

APPLICATION PROGRAMMING OF CORTEX M3/M4 **(09 Hours)**

Writing optimized ARM assembly/C code, Exception and fault handling routines, Handling floating point operations, Programming for DSP applications (such as Biquad filter, FIR filter, IIR filter, DFT, FFT etc.)

PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY **(30 Hours)**

(Total Contact Time: 45 Hours + 30 Hours = 75 Hours)

3.	**List of Practical:**
	1. Write assembly code to perform Arithmetic and Logical operations. 2. Write a assembly language code to multiply 32-bit data stored on R1 and R2 and 64-bit result will generated and stored into R3(H) and R4(L). Please refer the below figure to implement the same. 3. Write assembly language code to program STM32F4(ARM cortex M4) transfer the data with memory 4. Write Assembly language code to perform switch-case on STM32F4 5. Interface LED with STM32F4 & write embedded C code for the same 6. Interface Switch and LED with STM32F4 & write embedded C code for the same. 7. Interface 4x4 Keypad and LEDs with STM32F4 & write embedded C code for the same. 8. Interface LCD with STM32F4 & write embedded C code for the same. 9. Interface UART with STM32F4 & write embedded C code for the same. 10. Interface DAC and ADC with STM32F4& write embedded C code for the same 11. Mini Project using STM32F4
4.	**Books Recommended:**
	1. Joseph Yiu, "A definitive guide to the ARM-Cortex M3 and Cortex-M4 Processors", 3rd Ed., Newnes, 2013. 2. ShibuK.V., "Introduction to Embedded Systems", 1st Ed., TMH 2009. 3. Y. Zhu, "Embedded Systems with Arm Cortex-M3 Microcontrollers in Assembly Language and C" E-Man Press LLC, 2014. 4. A.N.Sloss, D.Symes and C. Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Elsevier, 2004. 5. ARM Cortex M4 Technical Reference Manual.
5.	**Reference Books:**
	1. DVS Murthy, Transducers and Instrumentation, PHI 2nd Edition2013 2. Gary Johnson / Lab VIEW Graphical Programing II Edition /McGraw Hill 1997.

B.Tech. III (VL) Semester V DATA COMMUNICATION NETWORKS EC321	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand the basic concepts and technologies used in networking.
CO2	Illustrate how data is transmitted over various mediums and assess the performance of these systems
CO3	Analyze the performance of various techniques and protocols in a given network topology, case study and problem solving as per given data.
CO4	Implement and simulate basic networking protocols using standard tools.
CO5	Create a local area network with specific requirements.

2. Syllabus:

DATA COMMUNICATION AND NETWORKING OVERVIEW **(08 Hours)**

Components of a Data Communication Network, Data Flow Types, Categories of topology and their comparison, Protocols and Standards: Need for Protocols and Standards.

OSI and TCP/IP Reference Models: Need of Protocol Layering, Layers, Functions of layers, and Protocol Stacks.

Transmission Media: Guided (Twisted Pair, Coaxial, Fiber Optic) vs. Unguided (Wireless, Satellite).

Performance Parameters: Latency, Packet Delivery Ratio, Throughput and Jitter

Switching Techniques: Circuit Switching, Packet Switching, and Virtual Circuit Switching.

Addresses: Physical Address (MAC Address), IP Addresses, Port Address, Specific Addresses

DATA LINK LAYER **(12 Hours)**

Data Link Layer Functions: Framing: Bit Orientated framing and Byte oriented framing.

Flow Control and Error Control: Simplest, Stop and Wait, Stop and Wait ARQ, Go back N and Selective repeat Protocols.

Medium Access Control (MAC): Channelization Protocols: FDMA, TDMA and CDMA, Controlled Access Protocols: Reservation, Polling and Token Passing and Random Access Protocols: Pure Aloha, Slotted Aloha, CSMA 1-persistent, non-persistent and p-persistent, CSMA/CD, CSMA/CA.

Networking Devices: Hubs, Switches, Bridge: Learning Bridge, Loop Problem in Learning Bridge, Routers, and Gateways.

High-Level Data Link Control (HDLC) Protocol

Wired Networks: IEEE 802.3 Standard (Ethernet) and Wireless Networks: IEEE 802.11 Standard.

NETWORK LAYER **(12 Hours)**

IPv4 Addressing: Classful and Classless Addressing, Subnetting, and Supernetting, Special Addresses: Network Address, Broadcast Address, Default Gateway Address, Private IP Addresses, Loopback Address, Link-Local Addresses, Multicast Addresses, Reserved Addresses, Private vs. Public IP addresses, Network Address Translation,

IPv6 Addresses: IPv6 Address Types, IPv6 Address Scope, Stateless Address Autoconfiguration.

	Unicast Routing Protocol: Static vs. Dynamic Routing, Intra-Domain Routing: Distance Vector Routing (RIP), Link State Routing (OSPF), Inter-Domain Routing: Path Vector Routing (BGP). IPv4 Protocol: Datagram Format and explanation of its fields. Address Resolution Protocol (ARP), Address Resolution Protocol (RARP), Internet Control Message Protocol (ICMP), Internet Group Management Protocol (IGMP)
	TRANSPORT LAYER **(6 Hours)**
	Transport Layer Protocols: UDP, TCP and SCTP Protocols and underlying concepts (Three-way handshaking, Congestion Control, Flow Control Techniques etc.)
	APPLICATION LAYER **(7 Hours)**
	Network Virtual Terminal (TELNET), File Transfer Protocol (FTP), Hyper Transfer Protocol (HTTP), HTTPS, Network Management - SNMP, Domain Name Server (DNS), URL, WWW, DHCP, BOOTP. Email Architecture: Simple Mail Transfer Protocol (SMTP), Post Office Protocol version 3 (POP3), Internet Message Access Protocol (IMAP).
	PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY **(30 Hours)**
	(Total Contact Time: 45 Hours + 30 Hours = 75 Hours)
3.	**List of Practical:**
	1. Study of basic TCP/IP network commands using Command Window/Terminal. 2. Write a SCILAB program to do Bit stuffing and De-Stuffing for all the type. 3. Write a SCILAB program to generate Cyclic Redundancy Check (CRC) and Hamming code for Error Correction and Detection. 4. Write a SCILAB program to find the shortest path between the Nodes among the given networks. 5. Write a SCILAB program to calculate the Bit Error Rate (BER) in data transmission. 6. Demonstrate the difference between a Bridge and a Router using Cisco Packet Tracer. 7. Simulate Routing Information Protocol for intradomain routing using Cisco Packet Tracer. 8. Set up a DNS server to translate domain names into IP addresses for network devices using Cisco Packet Tracer. 9. Simulate the Stop-and-Wait ARQ protocol for reliable data communication. 10. Simulate the Go-Back-N ARQ protocol for error and flow control. 11. Simulate a Complete Wired Network 12. Simulate a Complete Wireless Network.
4.	**Books Recommended:**
	1. Tanenbaum Andrew S., "Computer Networks", PHI, 5th Ed., 2011. 2. Stalling William, "Data and Computer Communications", PHI, 10th Ed., 2014. 3. Forouzan Behrouz A., "Data Communications and Networking", Tata McGraw-Hill, 5th Ed., 2013. 4. Gallager R. G. And Bertsekas D., "Data Networks", PHI, 2nd Ed., 1992. 5. Garcia Leon and Wadjaja I., "Communication Networks", Tata McGraw-Hill, 2nd Ed., 2004.
5.	**Reference Books:**
	1. Doug Lowe, Networking All-in-One for Dummies, 7ed, 2018.

B. Tech. III (VL) Semester V SEMICONDUCTOR DEVICE MODELLING EC 341	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe semiconductor device physics and equations used for deriving a model.
CO2	Demonstrate various carrier transport equations.
CO3	Analyze methods to form closed-form analytical models.
CO4	Evaluate the operation of semiconductor devices using numerical methods.
CO5	Develop models for novel semiconductor devices.

2. Syllabus

DEVICE PHYSICS **(03 Hours)**

Review of Semiconductor Physics: PN Junction diode, Heterojunctions, MOSFETS.

SEMICONDUCTOR CARRIER TRANSPORT EQUATIONS **(07 Hours)**

The Boltzmann model, Maxwell's Equations, The Classical Semiconductor Equations, Boundary Conditions, Generation and Recombination, and Thermal Conductivity and Heat Flow.

CLOSED-FORM ANALYTICAL MODELS **(08 Hours)**

Solution Techniques for the Semiconductor Equations, Closed-Form Analysis of the Semiconductor Equations, Analysis of a PN junction diode, Analysis of Field effect Transistor Operation, Analysis of MOSFET Operation and Limitations of Closed-Form Analyses

FINITE-DIFFERENCE METHOD **(06 Hours)**

Finite-Difference Schemes, Discretization of the Semiconductor Equations, Methods of Solving the Finite-Difference Equations, Boundary Conditions, and Examples of Finite-Difference Simulations.

SEMICLASSICAL TRANSPORT EQUATIONS **(06 Hours)**

Hot Electron Effects: The Hydrodynamic Semi-classical Semiconductor Equations, Examples of Hot Electron Modelling

SIMULATION OF HETEROJUNCTION DEVICES **(05 Hours)**

Semiconductor Equations for Heterojunctions, High Electron Mobility Transistors: Closed-Form Models and Numerical Models.

THE MONTE CARLO METHOD **(05 Hours)**

The Monte Carlo Method applied to Carrier Transport in Semiconductors: Equations of Motion, Energy Band Structure and Free Flight, and Scattering Mechanisms, Treatment of Results, and Applications of Monte Carlo Simulations.

	QUANTUM TRANSPORT THEORY	**(05 Hours)**
	Extension of Semiclassical Transport Concepts to Quantum Structures, Quantum mechanics – Basic Concepts, Application of Quantum Mechanics to Semiconductor Device Modelling, Quantum Transport Theory, and Applications of Quantum Transport Theory	
	Total Contact Time: = 45 Hours	
3.	**Books Recommended**	
	1. Snowden C.M., and, Snowden E., "Introduction to Semiconductor Device Modeling", World-Scientific, 1998. 2. Selberherr S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag, First edition, 1984. 3. Taur Y. and Ning T.H. "Fundamentals of Modern VLSI Devices, ", Cambridge University Press, Third Edition, 2021. 4. Vasileska D., Goodnick S. M., and Klimeck G., "Computational Electronics Semiclassical and Quantum Device Modeling and Simulation, CRC Press, 2010. 5. Sze S. M., Li Y., and Kwok K. Ng, "Physics of Semiconductor Devices", John Willey, Fourth Edition, 2021.	

B.Tech. III (VL) Semester V HARDWARE DESCRIPTION LANGUAGE VL343	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand the concept of structural, data flow and behavioral style of hardware description and model various delays
CO2	Implement register transfer and gate level Digital system circuits. Also, verify with HDL simulations, Sequential circuits and FSMs
CO3	Develop and implement combinational logic circuits such as mux, demux, encoder, decoder, adders using Verilog and VHDL.
CO4	Evaluate the synthesized hardware for area, power and speed
CO5	Design ALU, instruction decoder, FIFO using HDL

2. Syllabus

INTRODUCTION **(11 Hours)**

Basic Concepts Of Hardware Description Languages, Hierarchy, Concurrency, Logic And Delay Modeling, Structural, Data-Flow And Behavioral Styles of Hardware Description, Architecture Of Event Driven Simulators

VHDL – MODELLING AND ANALYSIS **(16 Hours)**

Syntax And Semantics Of VHDL, Variable And Signal Types, Arrays And Attributes, Operators, Expressions And Signal Assignments, Entities, Architecture Specification And Configurations, Component Instantiation, Concurrent And Sequential Constructs, Use Of Procedures And Functions, Examples of Digital Design Using VHDL

VERILOG – DIGITAL DESIGN AND SYNTHESIS **(18 Hours)**

Syntax And Semantics Of Verilog, Variable Types, Arrays And Tables, Operators, Expressions And Signal Assignments, Modules, Nets And Registers, Concurrent And Sequential Constructs, Tasks And Functions, Examples Of Design Using Verilog, Synthesis Of Logic From Hardware Description

(Total Contact Hours: 45)

3. Books Recommended

1. Bhaskar J.,"VHDL Primer",Pearson Education Asia, 3rd Edition, 2015
2. Perry D.,"VHDL",Tata McGraw-Hill, 4th Edition, 2017
3. Navabi Z.,"VHDL",McGraw Hill, 3rd Edition,2007
4. Palnitkar S.,"Verilog HDL: A Guide to Digital Design and Synthesis", Pearson, 2nd Edition, 2003
5. Bhaskar J.,"Verilog HDL Synthesis - A Practical Primer",Star Galaxy Publishing, 2018

B.Tech. III (VL) Semester V SENSORS AND TRANSDUCERS EC361	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Explain the different types of sensors and transducers with working principle.
CO2	Apply the concepts of sensors for various applications.
CO3	Analyze different sensors and transducers for various applications.
CO4	Evaluate the applications of sensors in measurements/instrumentation.
CO5	Design the basic sensors systems for different applications.

2. Syllabus:

INTRODUCTION **(05 Hours)**

General Concepts and Terminology, Definition of Transducer, Sensor and Actuator, Transducer/Sensor Classification, Criteria to Choose a Transducer/Sensor, Characteristics parameters of Sensors.

RESISTIVE TRANSDUCERS **(06 Hours)**

Resistive Potentiometers, Strain Gauges, Resistive Temperature Detectors, RTDs, PTD, Thermistors, Light-Dependent Resistors (LDRs), Resistive Hygrometers, Resistive Gas Sensors

INDUCTIVE AND MAGNETIC TRANSDUCERS **(06 Hours)**

Inductive Transducers: Self-inductive transducer, Mutual inductive transducers, Linear Variable Differential Transformer-LVDT Accelerometer, Applications of Inductive Transducers such as proximity sensors for position measurement, dynamic motion measurement, Magnetic Sensors: Sensors based on Hall Effect, Performance Characteristics and Applications.

CAPACITIVE TRANSDUCERS **(04 Hours)**

Working Principle of Capacitive Transducer, Variable Distance based Capacitive Transducers, Variable Area based Capacitive Transducers, Variable Distance based Capacitive Transducers, Calculation of sensitivities, Applications of Capacitive Transducers for the measurement of different physical and bio-analytes.

SELF-GENERATING TRANSDUCERS **(06 Hours)**

Principle of operation, construction, theory, advantages and disadvantages and applications of following transducers: Thermocouple, Piezo-electric transducer, Pyroelectric transducers, Photo-voltaic transducer and Electrochemical transducer.

OPTICAL AND ACOUSTIC TRANSDUCERS **(04 Hours)**

Principle of Optical fiber based sensors, Types of optical sensors, Applications of optical sensors and biosensors. Principle Acoustic transducers, SAW and IDT sensors, Applications of Acoustic transducers, Ultrasonic Sensor.

BIOSENSORS **(03 Hours)**

Principle of Biosensors, Performance Criteria of Biosensors, Types of Biosensors such as Electrochemical, Thermal, Resonant, Ion-sensitive, Optical etc. and its applications.

PRESSURE, FLOW AND LEVEL TRANSDUCERS **(07 Hours)**

Pressure Transducers Like U-tube manometer, Bourdon tube, Diaphragm and Bellows, Membranes And Thin Plates, Piezo-resistive, Capacitive Sensors, VRP Sensors, Pirani vacuum gauge Vacuum Sensors. Flow Transducers Like Differential Pressure, Orifice Plate Flow meter, Flow Nozzle, Hot Wire

	Anemometer, Ultrasonic Flow meter, Vortex Flow meter. Level Transducers Like Displacer, Float, Pressure Gages, Capacitive, Resistive, Ultrasonic type level measurements, Level Switch.	
	ADVANCEMENTS IN SENSORS AND TRANSDUCERS	**(04 Hours)**
	Sensors Used In Smartphone, Sensors Used In Smart city, Sensors For Robotics, MEMS and Nano Sensors, Smart and Integrated Sensors, IoT Applications.	
	(Total Contact Hours: 45)	
3.	**Books Recommended:**	
	1. S. Vijayachitra, “Transducers Engineering”, PHI Learning Pvt. Ltd., 1st Ed., 2016 2. Ghosh Arun K., “Introduction to Transducers”, PHI Learning Pvt. Ltd., 1st Ed., 2014 3. Patranabis D., "Sensors and Transducers", 2nd Ed., Prentice-Hall India, 2004. 4. Shawhney A. K., "A Course in Electrical and Electronic Measurements and Instrumentation", Dhanpat Rai & Sons, January 2021. 5. Alok Barua, “Fundamental of Industrial Instrumentation”, 1st Ed., Wiley India, 2011. 6. Jacob Fraden, "Handbook of Modern Sensors: Physics, Designs and Applications", 3rd Ed., Springer, 2004.	

B. Tech. III (VL) Semester VI ANALOG VLSI DESIGN VL302	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand Impact of MOS Device Parameters on Analog Circuit Design and the Analog Design Requirements.
CO2	Design and Analyze various CMOS Amplifiers, Differential Amplifiers, Current Source/Sink Circuitry.
CO3	Analyze various Op-amp topologies and compensation techniques.
CO4	Evaluate suitability of a specific topology of Analog Sub-Circuits / Biasing Circuits / Data Converters etc. for a particular application.
CO5	Investigate Switch Capacitor Circuits for filter design

2. Syllabus

ANALOG CMOS SUB-CIRCUITS	**(10 Hours)**
Small Signal Model For MOS, MOS Switch, MOS Resistors, Current Sink/Source, High Input Impedance Current Mirrors, Differential, Cascode And Current Amplifiers, Output Amplifiers, High Gain Amplifier Architectures	
CMOS OPERATIONAL AMPLIFIERS	**(09 Hours)**
Design of CMOS Operational Amplifiers, Telescopic Op-amp topologies, Compensation, Design of Two Stage Op-Amps, Cascode Op-Amps, Simulation And Measurement Techniques	
HIGH PERFORMACE CMOS OP-AMPS	**(07 Hours)**
Buffered Op-Amps, High Speed/Frequency Op-Amps, Differential Output Op-Amps, Micro Power Op-Amps, Low Noise And Low Voltage Op-Amps	
SWITCHED CAPACITOR FILTERS	**(09 Hours)**
Switched Capacitor Circuits: Design and Analysis, Switched Capacitor Amplifiers, Switched Capacitor Integrators, Z Domain Models, 1st And 2nd Order Switch Capacitor Filters, Higher Order Filters	
D/A AND A/D CONVERTERS	**(10 Hours)**
Sample And Hold Circuits. Characterization of DAC, Nyquist Rate, Parallel DAC, Extending Resolution Of Parallel DAC, Serial DAC, Characterization Of ADC, Serial ADC, High Speed ADC, Over Sampling Techniques	
	Total Contact Time: 45 Hours

3.	**List of Practical:**
	1. Obtain various V-I characteristics of PMOS and NMOS transistor. 2. Design and simulate single stage CS amplifier with different load 3. Design and simulate single stage CG and CD amplifier with different load 4. Design & Simulate following current mirrors topologies. 5. Simulate and evaluate CS amplifier with feedback. 6. Design and Simulate Cascode amplifier with following specifications: 7. Characterize and evaluate Differential amplifier with resistive load. 8. Realize 3-bit Charge Scaling DAC and find output voltage for all input combinations. 9. Design 4-bit R-2R ladder DAC using active and passive switches 10. Design and Simulate Differential amplifier with current mirror load for given specifications. 11. Design of uncompensated single stage telescopic op-amp. 12. Realize and evaluate folded cascade op-amp
4.	**Books Recommended:**
	1. John D. A. and Martin K., "Analog Integrated Circuit Design", 2nd Ed., Wiley, 2013 2. Razavi Behzad, "Design of Analog CMOS Integrated Circuit", Tata McGraw-Hill, 2nd Edition, 2017 3. Allen Philip and Holberg Douglas, "CMOS Analog Circuit Design", Oxford University Press, 3rd Edition, 2016 4. Gregorian R. and Temes G.C., "Analog MOS ICs for Signal Processing", Wiley 2008 5. Baker Jacob R., Harry W. Li and Boyce David E.,"CMOS: Circuit Design, Layout and Simulation", Wiley, Interscience, 3rd Edition, 2013

B.Tech. III (VL) Semester VI VLSI SYSTEM DESIGN VL304	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe systems levels issues related to interconnect and its solution.
CO2	Apply the system decompositions in data path and control path.
CO3	Analysis of sequential logic circuit design.
CO4	Evaluate various Timing issues and its solutions.
CO5	Design systems with shared memory architecture.

2. Syllabus:

INTERCONNECT **(12 Hours)**

The Wire, Interconnect Parameter, Electrical and Spice Wire Model, RLC Parasitic, Signal Integrity and High Speed Behavior Of Interconnects: Ringing, Cross Talk And Ground Bounce. Layout Strategies at IC And Board Level for Local and Global Signals, Power Supply Decoupling, Advance Interconnect Techniques. Clocking strategy.

SYSTEM HARDWARE DECOMPOSITION **(10 Hours)**

VLSI Design Flow, Mapping Algorithms into architectures, Data Path And Control Path, Register Transfer Level Description, Control Path Decomposition (Interfacing With FSM), Pitfalls of Decomposition, Critical Path and worst case timing analysis, Control Flow And Data Flow Pipelines, Communication Between Subsystems, Control Deadlocks. Concept of hierarchical system design; Data-path element: Data-path design philosophies, fast adder, multiplier, driver etc. Timing And Control Shared Memory Data Hazards And Consistency, Mutual Exclusion.

DESIGNING OF SEQUENTIAL LOGIC CIRCUIT **(10 Hours)**

Timing classification; Synchronous design; Self-timed circuit design; Clock Synthesis and Synchronization: Synchronizers; Arbiters; Clock Synthesis; PLLs; Clock generation; Clock distribution; Synchronous Vs Asynchronous Design, Static And Dynamic Latches And Registers, Design And Optimization Of Pipelined Stages, Timing Issues In Digital Circuits, Handling Multiple Clock Domains, Interface Between Synchronous And Asynchronous Blocks, Set-Up And Hold Time Violation, Concept Of Meta-Stability.

MEMORY SUBSYSTEM DESIGN **(13 Hours)**

Memory Architecture, Shared Memory Architecture, Data Hazards and Consistency, Mutual Exclusion

PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY **(30 Hours)**

Total Contact Time: = 45 Hours + 30 Hours = 75 Hours

3.	**List of Practical:**
	1. Introduction of IP Integrator. Implement the trigonometric function using CORDIC IP 2. Design and Simulate following using IP a) Single MAC , b) Parallel MAC, c) Serial MAC 3. Design and Implement Low Pass FIR filter 4. Debugging MAC unit in hardware using ILA core and viewing ILA probe data in the waveform viewer. RTL 2 GDSII (Standard Cell based Semi custom ASIC Flow) ● To study Logic synthesis: Using standard cell library and analysis of area, power, delay report. To obtain the design constraint file, LEC (Logic Equivalence Check), DFT (Design For Testability) insertion to verify the chip after fabrication, Gate-level netlist generation ● To study Place and Route (PnR): To place all the standard cells, Macros and I/O pads with minimal area, with minimal delay and Route based on Gate-level netlist, Floor Plan, Power Plan, Placement, CTS (Clock Tree Synthesis), and Routing , DRC (Design Rule Check) error, GDS-II file generation ● Signoff or Tapout : To fix the timing violations by post route simulation and a final layout file free from all the violations is streamed out in GDSII format 5. Topics for Mini Projects: Radix-4 Booth Multiplier, Parallel prefix adders, UART Hardware, I2C transceiver hardware, Divider, Square Root, CORDIC arithmetic, Control unit design for CPU Data path
4.	**Books Recommended**
	1. Rabaey Jan M., Chandrakasan Anantha and Borivoje Nikolic, "Digital Integrated Circuits (Design Perspective)", 2nd Ed., Prentice Hall of India, 2016 (Reprint). 2. Neil H. E. Weste, David. Harris and Ayan Banerjee,, “CMOS VLSI Design”, 4th Ed., Pearson Education, 2019 3. Smith M. J. S., "Application Specific Integrated Circuits", 1st Ed., Addison Wesley, 1999. 4. Dally W. J. and Poulton J. W., "Digital System Engineering", 1st Ed., Cambridge University Press, 1998. 5. Hall S. H., Hall G. W. and McCall J. A., "High Speed Digital System Design", 1st Ed., John Wiley & Sons, 2000. 6. Bakoglu H. B., "Circuit Interconnect and Packaging For VLSI", 1st Ed., Addison-Wesley, 1990. 7. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test principles And Architectures Design For Testability", 1st Ed., Morgan Kaufmann Publishers, 2006.
5.	**Reference Books**
	1. Bakoglu H. B., "Circuit Interconnect and Packaging For VLSI", 1st Ed., Addison-Wesley, 1990. 2. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test principles And Architectures Design For Testability", 1st Ed., Morgan Kaufmann Publishers, 2006.

B.Tech. III (VL) Semester VI REAL TIME SYSTEMS VL322	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Explain fundamental principles for programming of real time systems with time and resource limitations.
CO2	Describe the foundation for programming languages developed for real time programming.
CO3	Account for how real time operating systems are designed and functions.
CO4	Describe what a real time network is.
CO5	Use real time system programming languages and real time operating systems for real time applications.
CO6	Analyse real time systems with regard to keeping time and resource restrictions.

2. Syllabus:

INTRODUCTION TO REAL-TIME SYSTEMS **(10 Hours)**

Hard Versus Soft Real Time Systems, Reference Models of Real Time Systems, Operating System Services, I/O Subsystems, Network Operations Systems, Real Time Embedded Systems, Operating Systems Interrupt Routines in RTOS Environments, RTOS Task Scheduling Models, Interrupt Latency And Response Time, Standardization Of RTOS.

REAL-TIME SCHEDULING AND SCHEDULABILITY ANALYSIS **(10 Hours)**

Task, Process And Threads, Commonly Used Approaches To Real Time Scheduling, Clock-Driven Scheduling, Priority Driven Scheduling Of Periodic Tasks, Hybrid Schedules, Event Driven Schedules, Earliest Dead Line First (EDF) Scheduling, Rate Monotonic Algorithm (RMA), Real Time Embedded Operating Systems: Standard & Perspective, Real Time Operating Systems: Scheduling Resource Management Aspects,Quasi-Static Determining Bounds On Execution Times.

INTER-PROCESS COMMUNICATION AND SYNCHRONIZATION OF PROCESSES,TASKS AND THREADS **(06 Hours)**

Multiple Process in An Application, Data Sharing By Multiple Tasks And Routines Inter Process Communication.

REAL-TIME OPERATING SYSTEMS **(13 Hours)**

Handling Resources Sharing and Dependencies Among Real Time Tasks, Resource Sharing Among real Time tasks, Priority Inversion, Priority Inheritance Protocol (PIP), Highest Locker Protocol (HLP), Priority Ceiling Protocol (PCP), Different Types of Priority Inversion Under PCP, Important Features of PCP, Handling Task Dependencies, Real time communication, Real time systems for multiprocessor systems, Real-time databases.

COMMERCIAL REAL TIME OPERATING SYSTEMS **(06 Hours)**

Time Services, Unix As Real Time OS, Non-Primitive Kernel, Dynamic Priority Levels, Unix Based Real Time OS, Extension to the Traditional Unix Kernal, Host Target Approach, Preemption Point Approach, RT Linux, Windows CE as Real Time OS, Real Time POSIX Standard, MC/OS-II

PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY **(30 Hours)**

(Total Contact Time: 45 Hours + 30 Hours = 75 Hours)

3.	**List of Practical:**
	1. Concepts of Multi-threading using pThreads library 2. Semaphore, Mutual exclusion and Condition variable using pThreads 3. Data synchronization using pThreads. 4. Introduction to FreeRTOS and Target hardware 5. LED blinking using FreeRTOS library 6. UART transmission using FreeRTOS library 7. Multiple GPIOs and LED using FreeRTOS library 8. Implementation of Round-Robin algorithm using FreeRTOS 9. Implementation of EDF Algorithms using FreeRTOS 10. Implementation of RMA Algorithm using FreeRTOS 11. Implementation of Resource Access Control using FreeRTOS
4.	**Books Recommended:**
	1. Rajib Mall, “Real Time Systems Theory and Practice”, 1st Ed., Pearson Education, 2007. 2. Wayne Wolf, “Computers as Components: Principles of Embedded Computing System Design”, 2nd Ed., Morgan Kaufman, 2008. 3. Liu Jane, “Real-time Systems”, 1st Ed., PHI, 2000. 4. Albert M. K. Cheng, “REAL-TIME SYSTEMS Scheduling, Analysis, and Verification”, 1st Ed., Wiley Interscience, 2002. 5. Richard Zurawski, “Embedded Systems Handbook”, 1st Ed., CRC Taylor Francis, 2006.

B.Tech. III (VL) Semester VI VLSI ARCHITECTURES FOR DIGITAL SIGNAL PROCESSING EC324	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe DSP/ML algorithms using data flow graphs and various VLSI architectures for signal processing and Machine learning
CO2	Apply fast convolution methods for optimization.
CO3	Analyze critical path algorithm and strength reduction.
CO4	Evaluate signal processing/Machine Learning architectures based on area and power.
CO5	Design VLSI architectures for the signal processing/Machine Learning based on specifications.

2. Syllabus:

DSP CONCEPTS **(08 Hours)**

Linear system theory, DFT, FFT, DCT realization of digital filters. Typical DSP algorithms, DSP applications, Data flow graph presentation of DSP algorithm.

ARCHITECTURAL ISSUES **(10 Hours)**

Binary Adders, Binary multipliers, Multiply Accumulator (MAC) and Sum of Product (SOP). Pipelining and Parallel Processing, Retiming, Unfolding, Folding, Register Minimization Technique and Systolic architecture design, Coordic Architecture, Distributed Arithmetic Architecture

FAST CONVOLUTION **(09 Hours)**

Cook-Toom algorithm modified Cook-Toom algorithm, Winograd algorithm, modified Winograd algorithm, Algorithmic strength reduction in filters and transforms, DCT and inverse DCT, parallel FIR filters.

HARDWARE ARCHITECTURES FOR MACHINE LEARNING **(10 Hours)**

Architectural approaches for implementing DNN: reduced precision of operations and operands (floating point to fixed point, reducing the bit width, nonuniform quantization, and weight sharing), reduce number of operations and model size (compression, pruning, and compact network architectures). Advanced topics in ML hardware design

POWER ANALYSIS IN DSP SYSTEMS **(11 Hours)**

Scaling versus power consumption, power analysis, power reduction techniques, power estimation techniques, low power IIR filter design, Low power CMOS lattice IIR filter.

PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY **(30 Hours)**

(Total Contact Time: 45 Hours + 30 Hours = 75 Hours)

3.	**List of Practical:**
	1. Investigation in FIR Filter to Improve Power Efficiency and Delay Reduction. 2. Power Optimization of Single Precision Floating Point FFT Design Using Fully Combinational Circuits 3. Area-Time Efficient Scaling-Free CORDIC Using Generalized Micro-Rotation Selection 4. Design and Implementation of Adaptive filtering algorithm for Noise Cancellation in speech signal on FPGA 5. A Reconfigurable Overlapping FFT/IFFT Filter 6. High-Throughput Programmable Systolic Array FFT Architecture and FPGA Implementations 7. Hardware Implementation of Adaptive LMS Filter 8. Hardware implementation of Convolution Engine 9. Hardware implementation of Max Pool Layer 10. Hardware implementation of Quantized Neural Network 11. Mini Projects
4.	**Books Recommended:**
	1. Keshap K. Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, 1st Ed., John Wiley, 2007. 2. Keshab K. Parhi and Takao Nishitani, Marcel Dekker “Digital Signal Processing for Multimedia Systems”, 1st Ed., CRC Press, 1999. 3. U. Meyer-Baese, “Digital Signal processing with Field Programmable Arrays”, 4rd Ed., Springer, 2014. 4. Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel S. Emer, “Efficient Processing of Deep Neural Networks”, Springer Nature, 31 May 2022 5. Magdy A. Bayoumi, “VLSI Design Methodologies for Digital Signal Processing Architectures”, Springer US, 2012
5.	**Reference Books:**
	1. V. Sze, "Designing Hardware for Machine Learning," in IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 46-54, Fall 2017. 2. Maurizio Martina, “VLSI Architectures for Future Video Coding”, IET, 2019

B.Tech. III (VL) Semester VI FOUNDATION OF VLSI CAD VL342	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand CAD tools used for VLSI design and synthesis
CO2	Optimize the algorithms for portioning in the design process of Complex IC
CO3	Demonstrate capability of floor planning algorithm for CAD tool
CO4	Gather knowledge of Placement and Routing.
CO5	Understand Timing Closure

2. Syllabus:

INTRODUCTION TO VLSI CAD AND SYNTHESIS **(08 Hours)**

Intro to VLSI CAD & Logic Synthesis • Graph Theory & Optimization problems • Boolean Algebra • Boolean Function Representation & Manipulation: BDDs • Satisfiability & Graph Covering

NETLIST AND SYSTEM PARTITIONING **(08 Hours)**

Optimization Goals, Partitioning Algorithms: Kernighan-Lin (KL) Algorithm, Extensions of the Kernighan-Lin Algorithm, Fiduccia-Mattheyses (FM) Algorithm, A Framework for Multilevel Partitioning, Clustering, Multilevel Partitioning, System Partitioning onto Multiple FPGAs..

CHIP PLANNING **(08 Hours)**

Introduction to Floor planning, Optimization Goals in Floor planning, Floorplan Representations, Floor planning Algorithms, Pin Assignment, Power and Ground Routing

GLOBAL AND DETAILED PLACEMENT AND ROUTING **(13 Hours)**

Global Placement, Min-Cut Placement, Analytic Placement, Simulated Annealing, Modern Placement Algorithms, Legalization and Detailed Placement, The Global Routing Flow: Single-Net Routing; Rectilinear Routing; Global Routing in a Connectivity Graph; Finding Shortest Paths with Dijkstra's Algorithm; Finding Shortest Paths with A* Search, Full-Netlist Routing: Routing by Integer Linear Programming; Rip-Up and Reroute (RRR), Modern Global Routing: Pattern Routing; Negotiated Congestion Routing, Detailed Routing, Specialized Routing

TIMING CLOSURE **(08 Hours)**

Timing Analysis and Performance Constraints: Static Timing Analysis; Delay Budgeting with the Zero-Slack Algorithm, Timing-Driven Placement: Net-Based Techniques; Embedding STA into Linear Programs for Placement, Timing-Driven Routing: The Bounded-Radius, Bounded-Cost Algorithm; Prim-Dijkstra Tradeoff; Minimization of Source-to-Sink Delay, Physical Synthesis: Gate Sizing; Buffering; Netlist Restructuring

(Total Contact Time: 45 Hours)

3.	**Books Recommended:**
	1. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011. 2. Gary D. Hachtel, Fabio Somenzi, "Logic Synthesis and Verification Algorithms", Springer US, 1996 3. N. Shervani, "Algorithms for VLSI Physical Design Automation", 3rd Edn., Kluwer Academic Publishers, 1998 4. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw-Hill Education, 1994 5. S. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 1999
4.	**Reference Books:**
	1. Keshap K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", 1st Ed., John Wiley, 2007.

B.Tech. III (VL) Semester VI MEMORY TECHNOLOGY VL344	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand fundamental concepts of different memory technologies
CO2	Describe static RAM & dynamic RAM
CO3	Compare the various memory technologies
CO4	Analyze the various memory technologies
CO5	Design different advanced memory technologies

2. Syllabus:

INTRODUCTION TO MEMORY TECHNOLOGIES **(08 Hours)**

Memory organization and overview of memory technology: market, trends and technologies, Overview of volatile and non-volatile memory technology, Static Random-Access Memory (SRAM), Dynamic RAM (DRAM), 1T-1C architecture, Capacitorless-DRAM, On-chip memory, on-chip memory types.

STATIC RAM **(10 Hours)**

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

DYNAMIC RAM **(09 Hours)**

DRAMs, MOS DRAM Cell, Bi-CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

FLASH MEMORY **(08 Hours)**

Flash memory: NOR and NAND architecture, Poole Frenkel emission and Fowler-Nordheim tunneling, floating gate (FG) and charge-trap (CT) NAND flash, reliability, scaling and multi-bit capability (MLC) 3D NAND, BICS, TCAT, V-NAND, VG NAND Flash, reliability and MLC

ADVANCED MEMORY TECHNOLOGIES **(10 Hours)**

High-density Memory Packing Technologies, Emerging non-volatile memories (eNVM): Resistive RAM (RRAM), unipolar and bipolar stacks, oxygen vacancy and ionic transport, reliability and endurance, Phase change memory (PCM), Ferroelectric RAM (FeRAM), Gallium Arsenide (GaAs) FRAMs, Conductive Bridge RAM (CBRAM) and Spin-transfer Torque Magnetic RAM (STT-MRAM)

(Total Contact Hours: 45)

3. Books Recommended:

1. S. Yu, “Semiconductor Memory Devices and Circuits”, 1st Edition, CRC Press, 2022.
2. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing, and Reliability”, 1st Edition, Wiley IEEE, 2013
3. Kiyoo Itoh, “VLSI Memory Chip Design”, 1st Edition, Springer, 2001
4. N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd Edition. Pearson, 2006
5. Y. Nishi and Magyari-Kope, “Advances in non-volatile memory and storage technology”, Woodhead Publishing, 1st Edition, 2019.
6. Keeth, Baker, Johnson, and Lin, “DRAM Circuit Design: Fundamental and High-Speed Topics”, 2nd Edition, Wiley, IEEE 2007.

B.Tech. III (VL) Semester VI LOW POWER VLSI DESIGN VL346	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand the physics of power dissipation in CMOS
CO2	Estimate power that occurs due to various signal and circuit phenomena
CO3	Design low power CMOS circuits
CO4	Analyze VLSI Design Methodologies for achieving low power
CO5	Evaluate algorithms for power estimation and optimization

2. Syllabus

PHYSICS OF POWER DISSIPATION IN CMOS **(08 Hours)**

Submicron MOSFET, Gate induced drain leakage, Short circuit dissipation, Dynamic dissipation, Load capacitance, Low power limits: Hierarchy limits, fundamental limits, device limit, circuit limit, system limit

POWER ESTIMATION **(08 Hours)**

Probabilistic Techniques for Signal activity Estimation, Statistical Technique to estimate average power, Estimation of Glitch power, Power sensitivity analysis, Input vector compaction, Domino CMOS, Circuit reliability, High level power estimation, Estimation of maximum power

DESIGN OF LOW POWER CMOS CIRCUITS **(09 Hours)**

Circuit Design Styles, Leakage current and submicron device issues, Low voltage circuit design techniques, Multiple supply voltages

VLSI DESIGN METHODOLOGY FOR LOW POWER **(10 Hours)**

Low power physical design, Low power gate level design (Logic minimization, spurious transition reduction and precomputation based reduction), Low power architectural level design (parallelism, pipelining, distributed processing and power management) , Algorithmic level power reduction (switched capacitance and switching activity reduction

ALGORITHMS FOR LOW POWER **(10 Hours)**

Algorithms for power estimation (Gate level, Architectural level, Instruction level and bus switching activity), Power optimization: Algorithm transformations, minimizing memory access, Instruction selection/ordering and power management, Automated low power code generation, Codesign for Low power

Total Contact Time: = 45 Hours

3.	**Books Recommended**
	1. Kaushik Roy, Sharat C. Prasad, “Low-Power Cmos Vlsi Circuit Design”, John Wiley & Sons, 2009. 2. A. Bellamour, and M. I. Elmasri, “Low Power VLSI CMOS Circuit Design”, Springer US, 2012. 3. Anantha P. Chandrakasan and Robert W. Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, 2012. 4. Christian Piguet, “Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools”, Tayler and Francis (CRC), 2006. 5. Sung-Mo Kang and Y. Leblebici, “CMOS Digital Integrated Circuits”, Tata Mcgrag Hill, 3rd edition, 2003

B.Tech. III (VL) Semester VI IOT AND APPLICATIONS EC344	Scheme	L	T	P	Credit
		3	0	2	04

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Explain the key concepts and architecture of IoT systems.
CO2	Understand the hardware and software used in IoT systems.
CO3	Design and implement IoT-based applications using sensors, microcontrollers, and communication protocols
CO4	Evaluate the Performance of various protocols used in IoT systems.
CO5	Develop IoT systems for smart environments, such as smart cities, healthcare, and industrial automation.

2. Syllabus:

INTRODUCTION TO INTERNET OF THINGS **(06 Hours)**

Definition and characteristics of IoT, Evolution of IoT, key technologies, and drivers.
IoT architecture: Layers (perception, network, application).
Network topologies for IoT (star, mesh, peer-to-peer), Addressing schemes in IoT.
Applications of IoT: Overview of IoT applications in various domains (smart homes, smart cities, healthcare, agriculture, industry).

SENSORS, ACTUATORS, AND IOT DEVICES **(10 Hours)**

Overview of Sensors and Actuators: Types of sensors (temperature, pressure, humidity, light, proximity, motion, etc.), Types of actuators: motors, relays, servos.
Microcontrollers and Development Platforms: Introduction to popular IoT hardware platforms (Arduino, Raspberry Pi, ESP32), Integration of sensors and actuators with microcontrollers, Overview of communication interfaces: I2C, SPI, UART, GPIO.
Power Management in IoT Devices: Energy efficiency considerations in IoT systems.
Low-power communication technologies (BLE, LoRa, Zigbee).

IoT ARCHITECTURE AND PROTOCOLS **(12 Hours)**

Communication Models and IoT Protocols: Machine-to-Machine (M2M), Device-to-Device (D2D), Device-to-Cloud communication.
IoT Communication Protocols: Application Layer Protocols: MQTT, CoAP, HTTP/HTTPS. Transport Layer Protocols: TCP, UDP, MQTT-SN. Network Layer Protocols: IPv4, IPv6, 6LoWPAN. Data Link Layer Protocols: IEEE 802.15.4, LoRa, Bluetooth Low Energy (BLE), Zigbee, Wi-Fi.

CLOUD AND EDGE COMPUTING IN IoT **(10 Hours)**

Cloud Platforms for IoT: Overview of cloud services for IoT: AWS IoT, Google Cloud IoT, Microsoft Azure IoT Hub, Data storage, processing, and analytics using cloud platforms.
Edge and Fog Computing: Introduction to edge and fog computing in IoT, Role of edge devices for local processing, Hybrid cloud-edge architecture.
Data Analytics in IoT: Big data analytics for IoT-generated data, Data visualization tools for IoT.

IoT Applications and Case Studies **(7 Hours)**

Smart Homes and Buildings: IoT-based home automation (lighting, HVAC, security), IoT for smart energy management.
Smart Cities: IoT for urban planning (traffic management, smart parking, waste management), IoT for environmental monitoring.
Healthcare and Wearables: IoT applications in healthcare (remote patient monitoring, fitness tracking), Integration of wearable devices with healthcare systems.

	Industrial IoT (IIoT): IoT for industrial automation (predictive maintenance, supply chain management), IoT for smart manufacturing (Industry 4.0).	
	PRACTICAL WILL BE BASED ON THE COVERAGE OF THE ABOVE TOPICS SEPARATELY	**(30 Hours)**
	(Total Contact Time: 45 Hours + 30 Hours = 75 Hours)	
3.	**List of Practical:**	
	1. Familiarization with Arduino/Raspberry Pi/ESP32 and perform necessary software installation. 2. To interface LED and Buzzer with Arduino/Raspberry Pi/ESP32 and write a program to continuously turn ON LED for 1 second and turn it OFF for 2 seconds. 3. To interface Infrared sensor with Arduino/Raspberry Pi/ESP32 and write a program to turn ON LED at the sensor detection. 4. To interface temperature and humidity sensor with Arduino/Raspberry Pi/ESP32 and write a program to print temperature and humidity readings. 5. To interface LCD with Arduino/Raspberry Pi/ESP32 and write a program to print temperature and humidity readings on it. 6. To interface Bluetooth with Arduino/Raspberry Pi/ESP32 and write a program to send sensor data to smartphone using Bluetooth. 7. To interface Bluetooth with Arduino/Raspberry Pi/ESP32 and write a program to turn LED ON/OFF when 1/0 is received from smartphone using Bluetooth. 8. Write a program on Arduino/Raspberry Pi/ESP32 to upload temperature and humidity data to cloud. 9. Write a program on Arduino/Raspberry Pi/ESP32 to retrieve temperature and humidity data from cloud. 10. Write a program on Arduino/Raspberry Pi/ESP32 to publish temperature data to MQTT broker. 11. Write a program on Arduino/Raspberry Pi/ESP32 to subscribe to MQTT broker for temperature data and Print it. 12. Write a program to create TCP server on Arduino/Raspberry Pi/ESP32 and Respond with humidity data to TCP client when requested. 13. Write a program to create UDP server on Arduino/Raspberry Pi/ESP32 and respond with humidity data to UDP client when requested.	
4.	**Books Recommended:**	
	1. Pethuru Raj and Anupama C. Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", 1st Ed., CRC Press, 2017. 2. Arshdeep Bahga and Vijay Madisetti, "Internet of Things: A Hands-on Approach", 1st Ed., Universities Press, x 2014. 3. Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos and David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1st Ed., Academic Press, 2014. 4. Rahul Dubey, “An Introduction to Internet of Things: Connecting Devices, Edge Gateway, and Cloud with Applications”, 1st Ed., 2019. 5. Brian Russell and Drew Van Duren, “Practical Internet of Things Security”, Packt Publishing, 2016.	

B.Tech. III (VL) Semester VI SOLAR PHOTOVOLTAICS VL362	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Explain Solar Resource and Basics of Photovoltaic Systems.
CO2	Describe requirements for the efficient Photovoltaic Device Design and Processing.
CO3	Demonstrate different solar cell fabrication and characterization techniques.
CO4	Explain and analyze the Current and Emerging PV technologies, and PV Module related concepts.
CO5	Design the Solar Photovoltaic Devices.and PV Modules

2. Syllabus:

INTRODUCTION TO SOLAR PHOTOVOLTAICS **(04 Hours)**

Solar Resource, Solar Energy Conversion Technologies, Need of Solar PV, Prospects of PV technology.

FUNDAMENTALS OF SOLAR CELLS **(09 Hours)**

Light Absorption, Charge Excitation, Charge Drift/Diffusion, Charge Separation, Charge Collection, PN junction diodes: Dark IV, illuminated IV, Device Performance parameters: Short Circuit Current, Open Circuit Voltage, Fill Factor, Efficiency, Series/ Shunt Resistance, Factors affecting the performance parameters, Detailed Balanced Limit.

FABRICATION AND CHARACTERIZATION OF SOLAR CELLS **(10 Hours)**

Solar Cell Fabrication:
Vacuum Based Deposition Techniques: Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD): Sputtering, Electron Beam Evaporation, Pulsed Laser Deposition, Atomic Layer Deposition, Molecular Beam Epitaxy.
Solution Based Deposition Techniques: Electrodeposition, Spin Coating, Layer-by Layer Deposition, Printing, Colloidal Synthesis.
Solar Cell Characterization:
Solar Simulator, Quantum Efficiency Measurement, Secondary Ion Mass Spectroscopy, XPS/UPS, FESEM, Energy Dispersive X-Ray Spectroscopy, Photo-Luminescence

COMMERCIAL AND EMERGING TECHNOLOGIES IN SOLAR CELLS **(10 Hours)**

Silicon PV Technology, Chalcopyrite/ Kesterite Solar Cells, Organic Photovoltaics, Dye Sensitized Solar Cells, Perovskite Solar cells, Transparent Photovoltaic Devices, Flexible PV Devices, Multijunction Devices, Concentrator Solar Cells.

CUTTING-EDGE THEMES AND PV MODULES **(07 Hours)**

Light manipulation in PV Devices: Plasmonic Integration, Surface Texturing, Spectrum Splitting Techniques.Module Design, Interconnection effects, Temperature effects, Lifetime of PV modules, Module measurement.

PV DEVICE MODELING **(05 Hours)**

Basics of Solar Cell Device Modeling, Thin-Film Solar Cell Device Modeling: Hands-on with an Open Source Tool, Modeling of PV Modules.

(Total Contact Hours : 45)

3.	**Books Recommended:**
	1. Martin A. Green, “Solar Cells: Operating Principles, Technology and System Applications”,, Prentice-Hall, 1986. 2. Jenny Nelson, “The Physics of Solar cells”, World Scientific, 2003. 3. Smets Arno et al., “Solar Energy Fundamentals, Technology, and Systems”, UIT Cambridge. 2013 4. D. K. Schroder, “Semiconductor Material and Device Characterization”, Wiley Interscience, 2006 5. Konrad Mertens, “Photovoltaics Fundamentals, Technology, and Practice”, Wiley, 2018, 6. J. Poortmans and V. Arkhipov, “Thin Film Solar Cells: Fabrication, Characterization and Applications”, Willey, 2006.
4.	**Additional Resources:**
	1. Antonio Luque, Steven Hegedus, “Handbook of Photovoltaic Science and Engineering”, Wiley, 2011 Relevant Journal and Conference publications.

B.Tech. III (VL) Semester VI SEMICONDUCTOR PACKAGING VL364	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand fundamental concepts of different package manufacturing processes
CO2	Describe different semiconductor components and package tests
CO3	Demonstrate electrical and physical failure analysis
CO4	Identify different semiconductor package materials
CO5	Comply industrial quality and statistical process control

2. Syllabus:

PACKAGE MANUFACTURING PROCESSES **(08 Hours)**

Packaging Assembly Technology, Wafer Thinning, Dicing, Die Attach, Wire bonding, Flip Chip process, Flux Cleaning, Under fill, Encapsulation, Laser Marking, Solder Ball Attach, Reflow, Singulation, IC Packaging Toolsets & equipment operation, clean room operations

SEMICONDUCTOR COMPONENT AND PACKAGE TEST **(10 Hours)**

Overview of Testing methodologies, components tested & their characteristics, Challenges in testing, Types of Testers (Automated test Equipment & Benchtop Testers), Components & Subsystems of Testers, Principles of Functional Testing, Parametric/ Boundary Scan /In-Circuit Test/ Flying Probe Test, Test Data Analysis, Design for Testability & Tester Calibration & Maintenance, Future Trends

ELECTRICAL AND PHYSICAL FAILURE ANALYSIS **(09 Hours)**

Package failure modes, Failure detection mechanisms, Failure analysis tools, Test programs debugging, Data Analytics, ESD & EMI Management

SEMICONDUCTOR PACKAGE MATERIALS AND QUALIFICATION **(09 Hours)**

Reliability testing & qualification- MST/MSL, TC/TS, HAST & uHAST, Mold Compounds (Moldability), Underfill Materials, Die Attach Adhesives & Films, Substrate Technology, Bonding Wire, Solder & Dielectric materials

INDUSTRIAL QUALITY AND STATISTICAL PROCESS CONTROL **(09 Hours)**

Quality Control Plan (QCP) & Quality Management System (QMS), Incoming Material Inspection, In-Line Quality, Measurement System Analysis, Statistical analysis methods, Statistical Process Control (SPC), Fault Detection Control (FDC), Run-to-Run Control (R2R), Auto Defect

(Total Contact Hours: 45)

3. Books Recommended:

1. Hwaiyu Geng, “Semiconductor Manufacturing Handbook”, 2nd Edition, McGraw-Hill Education, 2017
2. Gary S. May and Costas J. Spanos, “Fundamentals of Semiconductor Manufacturing and Process Control”, 1st Edition, Wiley-IEEE Press, 2006
3. Peter Van Zant, “Microchip Fabrication: A Practical Guide to Semiconductor Processing”, 6th Edition, McGraw-Hill Professional, 2013
4. George Harman, “Wire Bonding in Microelectronics”, 3rd Edition, McGraw-Hill, 2010
5. Andrea Chen and Randy Hsiao-Yu Lo, “Semiconductor Packaging: Materials Interaction and Reliability”, CRC Press, 1st Edition, 2017