Department of Electronics Engineering

Proposed Revised Curriculum Structure as per NEP2020

B. Tech. Electronics and VLSI Engineering

Sr. No.	Subject	Code	Schemes	Credits	Notional hours
Seventh Semester					
1.	**Elective – V**	VL4XX	3-0-0	03	55
2.	**Elective – VI**	VL4XX	3-0-0	03	55
3.	**Elective – VII**	VL4XX	3-0-0	03	55
4.	**Elective – VIII**	VL4XX	3-0-0	03	55
5.	**Mandatory core** **Project Phase-III**	VL401	0-0-16	08	250
	Minimum Credit Requirement		**Total**	**20**	**470**
6	**Minor / Honors (M/H#4)**	**EC4AA**	**3-0-2**	**4/5**	**70/85**
Eighth Semester					
1	**Mandatory core** Internship training in Industry /Research Organization/ Academic Institute	VLP08	0-0-40	20	800 (20x40)
			Total	**20**	**800**
			Minimum Requirement	**20**	**800**
			Minimum Credit Requirement of full the program (Total)	**165**	**3810**

***NPTEL, SWAYAM and other Massive Open Online Courses (MOOC) approved by DAAC. As per 66th IAAC, Dated 20th March 2024, Resolution No. 66.34 and 61st Senate resolution No. 4, 25th April, 2024**

Subject Pool:

B. Tech. EVL Elective -V, VI, VII, VIII (3-0-0)				
Sr. No.	**Subject**	**Code**	**Scheme**	**Credits**
1	Testing and Verification of VLSI Circuits	VL421	3-0-0	3
2	UAV Avionics	VL423	3-0-0	3
3	Processor Architecture	VL425	3-0-0	3
4	Nanoelectronics	VL427	3-0-0	3
5	Robotics Systems	VL429	3-0-0	3
6	Quantum Computing	VL431	3-0-0	3
7	Secure Hardware	VL433	3-0-0	3
8	Biomedical Instrumentation	VL435	3-0-0	3
9	SoC Design	VL437	3-0-0	3
10	CMOS RF IC Design	VL439	3-0-0	3
11	Analog Mixed Signal IC Design	VL441	3-0-0	3
12	Hardware Architectures for Deep Learning	VL443	3-0-0	3
13	Error Correcting Coding	EC427	3-0-0	3
14	Deep Learning	EC435	3-0-0	3

B.Tech. IV (VL) Semester VII TESTING AND VERIFICATION OF VLSI CIRCUITS VL421	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand test patterns required to detect faults in a circuit
CO2	Demonstrate the testability of a circuit
CO3	Implement methods/techniques to improve the testability of digital circuits
CO4	Analyse Logic BIST circuits
CO5	Design the formal verification techniques

2. Syllabus

INTRODUCTION **(08 Hours)**

Scope Of Testing And Verification In VLSI Design Process, Issues In Test And Verification Of Complex Chips, Embedded Cores And SOCs

VLSI TESTING OF FAULT MODELS **(20 Hours)**

Fundamentals Of Automatic Test Pattern Generation, Design For Testability, Scan Design, Test Interface And Boundary Scan, System Testing and Test For SOC, Delay Fault Testing

Mu TESTING OF LOGIC AND MEMORIES **(10 Hours)**

Test Automation, Design Verification Techniques Based On Simulation, Analytical And Formal Approaches

VERIFICATION **(07 Hours)**

Functional Verification, Timing Verification, Formal Verification, Basics of Equivalence Checking And Model Checking, Hardware Emulation

(Total Contact Hours: 45)

3. Books Recommended

1. Bushnell M. and Agrawal V. D.,"Essentials Of Electronic Testing For Digital, Memory And Mixed-Signal VLSI Circuits", BS Publication,2015.
2. Abramovici M., Breuer M. A. and Friedman A. D.,"Digital Systems Testing And Testable Design",IEEE Press,1990.
3. Erik Seligman, Tom Schubert and M V Achutha Kiran Kumar, " Formal Verification An Essential Toolkit for Modern VLSI Design ", Morgan Kaufmann Publisher, 2023
4. Rashinkar P., Paterson and Singh L.,"System-On-A-Chip Verification-Methodology And Techniques",Kluwer Academic Publishers,2001.
5. Neil H. E. Weste and David Harris,"Principles Of CMOS VLSI Design",Addison Wesley, 3rd Edition,2004

B.Tech. IV (VL) Semester VII UAV Avionics System VL423	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe avionics components' working and interfacing
CO2	Relate for different avionics components and their interfacing
CO3	Illustrate the data communication between different avionics components
CO4	Explain GNSS signal processing flow in SoCs
CO5	Design and develop basic IPs and codes in SoC for GNSS receiver and communication transceiver
CO6	Implement system design for positioning of drones using SoCs

2. Syllabus:

Working of UAV Avionics systems **(14 Hours)**

Electronic Speed Controllers, Drone Motors, Ranging Sensors: Light detection and ranging (LiDAR), Laser detection and ranging (LADAR), Synthetic Aperture radar (SAR), Homing Radar, Positioning and Motion Sensors: Gyroscope, accelerometer, magnetometer; Pressure sensor, velocity sensor, Current and Voltage sensors, DC-DC Converters, Telemetry Communication Modules, Remote Servo Control Modules, Flight controller and mission controller onboard computer.

UAV Embedded Controller and Software **(14 Hours)**

Peripheral protocols like I2C, UART, and SPI; Sensor Interfacing: Accelero/Gyro/Magneto-meter module, Ultrasonic distance sensors, Infrared distance sensors, Lidar, pressure sensor, velocity sensor; Actuator Interfacing: BLDC motor, Servo motor, Solenoid Valve, Encoder DC motor, Gimble; Battery management System interfacing, Flight control software, Mission Control software, GNSS module interfacing, Robotic Motion peripheral interfacing: Motors, Motor Drivers, Motor Shields, ADC, DAC and PWM, Camera Interfacing, remote data logging, Introduction to ROS, Gazebo, and Mission Planner.

SoC-based GNSS receiver **(11 Hours)**

Introduction to SoC with RF front ends, Example of SoC designs, architecture of Processor subsystem and Programmable logic sections, data interchange between PS and PL, Implementation of control IPs for PL section including controlling RF front-end and digital control and data channels, FPGA based GNSS receiver Acquisition and Tracking algorithms, PL section system design and integration, Interface design between PL and PS, Implementation of control routines in PS section, AXI-based programming to control PS from PL section, testing of PL and PS section design, PS-PL integrated based band signal processing for GNSS receiver.

SoC-based Telemetry module **(6 Hours)**

Basics of telemetry transceiver design, radio communication aspect of the transceiver, Implementation of RF signal transmitter and receiver in PL section, Implementation of modulator and demodulator in PL section, DMA controller implementation for data exchange between PS and PL, Implementation of PL routines to get send/receive data between PS/PL and UART interface of PS section, testing of telemetry module.

(Total Contact Time: 45 Hours)

3.	**Books Recommended**
	1. Reg Austin, “Unmanned Aircraft Systems”, 1st Edition, Willy Publication 2011 2. R.P.G. Collinson, “Introduction to Avionics Systems”, 3rd Edition Springer Dordrecht Heidelberg London New York 2013 3. Andey Lennon, “Basics of R/C Model Aircraft Design”, 1st Edition, 1996, Model Airplane News Publication 4. John Baichtal, Building your own Drone: A begginers’ Guide to Drones,UAVs, and ROVs, 2015, 1st Edition. 5. Clive Max Maxfield, “The Design Warrior’s Guide to FPGAs”, 1st Edition, Newnes, Elsevier, Oxford OX2 8DP, UK
4.	**Reference Material**
	1. https://docs.xilinx.com/v/u/en-US/dh0050-zynq-7000-design-overview-hub 2. https://xilinx.github.io/video-sdk/v1.5/c_apis.html 3. https://digilent.com/reference/vivado/getting-started-with-ipi/2018.2 4. https://www.dgca.gov.in/digigov-portal/?dynamicPage=dynamicPdf/130650715&maincivilAviationRequirements/6/0/viewDynamicRulesReq

B.Tech. IV (VL) Semester VII PROCESSOR ARCHITECTURE VL425	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Discuss different processor architectures and system-level design processes.
CO2	Demonstrate the components and operation of a memory hierarchy and the range of performance issues influencing its design.
CO3	Analyze the organization and operation of current generation parallel computer systems, including multiprocessor and multicore systems.
CO4	Evaluate the principles of I/O in computer systems, including viable mechanisms for I/O and secondary storage organization.
CO5	Develop systems programming skills in the content of computer system design and organization.

2. Syllabus:

COMPUTER ABSTRACTIONS AND TECHNOLOGY **(04 Hours)**

Technologies for building processors and memory, Performance, Power wall, the switch from uniprocessors to Multiprocessors.

INSTRUCTION SET ARCHITECTURE OF 64-BIT RISC-V **(08 Hours)**

RISC-V addressing modes, instruction types, logical operations, instructions for making decisions, supporting procedures, RISC-V addressing for Wide Immediate and addresses, parallelism and instructions, comparison with MIPS and x86 Architectures.

PIPELINING **(11 Hours)**

An overview of pipelining, pipelined data-path and control, Data hazards: Forwarding versus Control, Control hazards, Exceptions, Parallelism via instructions, Real stuff: ARM CortexA53 and Intel Core i7 Pipelines, Case study: ILP and matrix multiply.

PARALLEL PROCESSORS **(13 Hours)**

Parallel programs, Flynn's taxonomy, Hardware multithreading, multicore and shared memory multiprocessors, Graphics processing units, Clusters and message passing multiprocessors, Multiprocessor networks, Benchmarking of Intel Core i7 960 and NVIDA Tesla GPU, Case study: Multiprocessors and matrix multiply, Cache coherence, Advanced Cache optimizations, Real stuff: The ARM Cortex-A53 and Intel Core i7 memory hierarchy, Case study: Cache blocking and matrix multiply.

STORAGE AND INTERCONNECTION **(09 Hours)**

The basic principles of interconnection network design, On-Chip Interconnection Network, Router Architecture, Network interface design, Case Study: NoC

(Total Contact Time: 45 Hours)

3.	**Books Recommended:**
	1. David A. Patterson, John L. Hennessy, “Computer Organization and Design: The Hardware Software Interface [RISC-V Edition]”, The Morgan Kaufmann Series in Computer Architecture and Design, 2017 2. John L Hennessy, “Computer architecture: a quantitative approach”, 6th Ed., Morgan Kaufmann Publishers, 2019 3. Leander Seidlitz, "RISC-V ISA Extension for Control Flow Integrity", Technische Universität München, 2019 4. Andrew Waterman, KrsteAsanović, The RISC-V Instruction Set Manual: Volume I: User-Level ISA, riscv.org, 2017 5. Andrew Waterman, KrsteAsanović, The RISC-V Instruction Set Manual: Volume II: Privileged Architecture, riscv.org, 2017
4.	**Reference Book:**
	1. William James Dally, Brian Patrick Towles, “Principles and Practices of Interconnection Networks”, Morgan Kaufmann, Year: 2004 2. Bernard Goossens, “Guide to Computer Processor Architecture: A RISC-V Approach, with High-Level Synthesis”, Springer Nature, 2023

B.Tech. IV (VL) Semester VII NANOELECTRONICS VL427	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Define various carrier transport mechanisms, properties of semiconductor materials, and novel devices using mathematical equations.
CO2	Describe the physics needed for special classes of nanoelectronic devices and their applications.
CO3	Illustrate the working of various nanoelectronic devices.
CO4	Analyse various nanoelectronic devices.
CO5	Design novel devices, processes and applications based on them.

2. Syllabus

FUNDAMENTALS OF NANOSCALE PHYSICS **(12 Hours)**

Top-Down and Bottom-Up Approach, Potential of Nanotechnology and Nanoelectronics, Classical Particles, Quantum Mechanics of Electrons, Free and Confined Electrons, Quantum Structures.

BAND THEORY OF SOLIDS **(09 Hours)**

Electrons in Periodic Potential, Kronig-Penney Model of Band Structure, Band Theory of Solids, Graphene and Carbon Nanotubes.

TUNNEL JUNCTION AND APPLICATIONS OF TUNNELING **(06 Hours)**

Tunnelling Through a Potential Barrier, Potential Energy Profiles for Material interfaces, Applications of Tunnelling: Field Emission, Gate-Oxide Tunnelling and Hot Electron Effects in MOSFETS, STM and Double Barrier Tunnelling, and The Resonant Tunnelling Diode.

COULOMB BLOCKADE AND THE SINGLE-ELECTRON TRANSISTOR **(06 Hours)**

Coulomb Blockade: Coulomb Blockade in a Nanoscale capacitor, Tunnel Junctions, Tunnel Junction Excited by a Current Source, and Coulomb Blockade in Quantum dot circuit, Single-Electron Transistor.

QUANTUM STRUCTURES **(12 Hours)**

Quantum Wells, Quantum Wires and Quantum Dots, Ballistic Transport and Spin Transport.

Total Contact Hours: 45 Hours

3. Books Recommended

1. Hanson, G. W., “Fundamentals of Nanoelectronics”, 1st Ed., Pearson Education, 2009.
2. Rogers, Pennathur and Adams, “Nanotechnology: Understanding Small Systems”, CRC Press, Tayler and Francis Group, 2008.
3. Mahalik N. P., “Micromanufacturing and Nanotechnology”, Springer, 2006
4. Kohler and Fritzsche, “Nanotechnology: An Introduction ToNanostructuring Techniques”, 1st Edition, 1st Reprint, Wiley-VCH, 2004.
5. Fahrner W. R. (Ed),“Nanotechnology And Nanoelectronics: Materials, Devices, Measurement Techniques”, Springer Publications, 2005.

B.Tech. IV (VL) Semester VII ROBOTICS SYSTEMS VL429	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe kinematics and dynamics of robotic system,
CO2	Estimate state of robotics system using Gaussian filters,
CO3	Compare approaches for robot motion planning and navigation,
CO4	Analyze probabilistic mathematics for robotic control, and
CO5	Design and control open chain robotics arms.

2. Syllabus

Basics of Robotics **(10 Hours)**

Configuration space, Degrees of freedom, Robotics joints, Grubler's formula, Configuration space topology, Velocity constraints, Task space and workspace, Vectors in different reference frames, Rigid body motion in plane, Rotation matrice, Angular and linear velocities, Exponential coordinates of rotation, Rodrigues' formula, Transformation matrices, Spatial and body twists, Wrenches.

Kinematics of Robots **(08 Hours)**

Open chain forward transformation kinematics, Product of exponential formula, computing open chain end-effector transformation, Open chain forward velocity kinematics, Jacobian, Manipulator ellipsoid, Manipulator Jacobian, Space and body Jacobian, Inverse transformation kinematics of 6R-PUMA Arm, Euler Angles, Newton-Raphson method, inverse velocity kinematics using Jacobian.

Dynamics of Robots **(08 Hours)**

Lagrangian Dynamics: Formulation for open chain dynamics, Derivation for 2-R open chain, mass matrix, Coriolis and centripetal terms, Generalized Lagrangian dynamics for n-link open chain, Newton Euler Dynamics: Classical formulation of wrench for single rigid body, Euler's equation, Inertia matrix, Inertia matrix in rotated and translated frames, Spatial inertia matrix, spatial momentum, Lie bracket of twist, Inverse Newton Euler dynamics for open chain derivation and algorithm.

Planning and Navigation **(08 Hours)**

Trajectory generation: P2P trajectories, Polynomial via point trajectories, Time optimal time scaling, Motion Planning: types, properties, and methods, Configuration space obstacles' localization and collision detection, Graph and trees, Grid method path planners, Sampling method path planners.

Probabilistic Robotics **(11 Hours)**

Basics: Revisiting basics of probability, Environment interaction, Probabilistic generative laws, Belief distributions, Bayes filters, Kalman filter (KF): theory and algorithm, derivation of KF, Extended Kalman filter (EKF): Linearization via Taylor expansion, EKF algorithm, Unscented Kalman Filter (UKF): Linearization Via the unscented transform, UKF algorithm, Information filter (IF): Canonical parameterization, IF algorithm, derivation of IF, Extended Information filter (EIF): Algorithm, Derivation of EIF.

(Total Contact Hours: 45)

3. Books Recommended:

1. Robert F. Stengel, "Robotics and Intelligent Systems: A Virtual Reference Book", Princeton University, Princeton, NJ, September 12, 2017

	2. Alonzo Kelly, Mobile Robotics: Mathematics, Models, and Methods, Cambridge University Press, 2013. 3. Kevin M. Lynch and Frank C. Park, Modern Robotics: Mechanics, Planning, and Control, Cambridge University Press, 2017 4. Sebastian Thrun, Wolfram Burgard, Dieter Fox, Probabilistic Robotics, MIT Press, 2005. 5. Steven M. LaValle: Planning Algorithms. Cambridge University Press, 2006

B.Tech. IV (VL) Semester VII QUANTUM COMPUTING VL431	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course, students will be able to:

CO1	To describe the basics of quantum computing
CO2	To distinguish between various types of qubits
CO3	To manipulate qubits using quantum gates
CO4	To analyse quantum algorithms
CO5	To understand and design quantum computers

2. Syllabus:

QUANTUM MECHANICS FOR QUANTUM COMPUTING **(12 Hours)**

Linear Algebra, The postulates of Quantum mechanics, The density operator, The Schmidt decomposition and purifications, Qubits And The Framework Of Quantum Mechanics, Models for computation, The analysis of computational problems.

QUANTUM CIRCUITS **(12 Hours)**

Quantum algorithms, Single qubit operations, Controlled operations, Measurement, Universal quantum gates, Simulation of quantum systems.

COMPONENTS FOR QUNATUM COMPUTING **(09 Hours)**

Different types of Qubits and their operation, Practical Quantum gates, Quantum Registers, Quantum Memory etc.

QUANTUM COMPUTERS **(12 Hours)**

Guiding principles, Conditions for quantum computation, Quantum Hardware: Harmonic oscillator quantum computer, Optical photon quantum computer, Optical cavity quantum electrodynamics, Ion traps, Nuclear magnetic resonance, other implementation schemes.

(Total Contact Hours: 45)

3. Books Recommended:

1. Michael A. Nielsen, Isaac L. Chuang, "Quantum Computation and Quantum Information: 10th Anniversary Edition", Cambridge University Press; 1st edition, 2011
2. P Kaye, R Laflamme and M Mosca, "An Introduction to Quantum Computing", Oxford University Press, 2007
3. David McMahon, "Quantum computing explained", Wiley-interscience, John Wiley & Sons, Inc. Publication 2008
4. P. Krantz, M. Kjaergaard , F. Yan, T.P. Orlando , S. Gustavsson and W. D. Oliver, "A Quantum Engineer's Guide to Superconducting Qubits", 2019
5. Arthur O. Pittenger, "An Introduction to Quantum Computing Algorithms", Birkhäuser Boston, 2012
6. David J. Griffiths, "Introduction to Quantum Mechanics", 3rd Edition, Cambridge University Press 2018

B.Tech. IV (VL) Semester VII SECURE HARDWARE VL433	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Identify different hardware security primitives
CO2	Discuss the side-channel attacks on hardware
CO3	Employ testability and verification for secure hardware
CO4	Analyse the modern IC design and manufacturing practices
CO5	Relate hardware trojans and infrastructure security

2. Syllabus:

USEFUL HARDWARE SECURITY PRIMITIVES: (06 Hours)

Cryptographic Hardware and their Implementation, Optimization of Cryptographic Hardware on FPGA, Physically Unclonable Functions (PUFs), PUF Implementations, PUF Quality Evaluation, Design Techniques to Increase PUF Response Quality

SIDE-CHANNEL ATTACKS ON CRYPTOGRAPHIC HARDWARE (08 Hours)

Basic Idea, Current-measurement based Side-channel Attacks (Case Study: Kocher's Attack on DES), Design Techniques to Prevent Side-channel Attacks, Improved Side-channel Attack Algorithms (Template Attack, etc.), Cache Attacks..

TESTABILITY AND VERIFICATION OF CRYPTOGRAPHIC HARDWARE: (06 Hours)

Fault-tolerance of Cryptographic Hardware, Fault Attacks, Verification of Finite-field Arithmetic Circuits

MODERN IC DESIGN AND MANUFACTURING PRACTICES AND THEIR IMPLICATIONS (10 Hours)

Hardware Intellectual Property (IP) Piracy and IC Piracy, Design Techniques to Prevent IP and IC Piracy, Using PUFs to prevent Hardware Piracy, Model Building Attacks on PUFs (Case Study: SVM Modeling of Arbiter PUFs, Genetic Programming based Modeling of Ring Oscillator PUF)

HARDWARE TROJANS: (08 Hours)

Hardware Trojan Nomenclature and Operating Modes, Countermeasures Such as Design and Manufacturing Techniques to Prevent/Detect Hardware Trojans, Logic Testing and Side-channel Analysis based Techniques for Trojan Detection, Techniques to Increase Testing Sensitivity

INFRASTRUCTURE SECURITY: (07 Hours)

Impact of Hardware Security Compromise on Public Infrastructure, Defense Techniques (Case Study: Smart-Grid Security)

(Total Contact Time: 45 Hours)

3.	**Books Recommended:**
	1. Ahmad-Reza Sadeghi and David Naccache (eds.): Towards Hardware-intrinsic Security: Theory and Practice, Springer, 2010 2. Ted Huffmire, Cynthia Irvine, Thuy D. Nguyen, Timothy Levi , Ryan Kastner, Timothy Sherwood, "Handbook of FPGA Design Security", Springer, 2010. 3. Stefan Mangard, Elisabeth Oswald, Thomas Popp: "Power analysis attacks - revealing the secrets of smart cards", Springer, 2007. 4. Mark Joye and Michael Tunstall, "Fault Analysis in Cryptography", 2012 5. D. Mukhopadhyay and R. S. Chakraborty, "Hardware Security: Design, Threats and Safeguards", CRC Press, 2014
4.	**Reference Books:**
	1. A. Das and C. E. Veni Madhavan, "Public-Key Cryptography: Theory and Practice", Pearson Education Asia, 2009

B.Tech. IV (VL) Semester VII BIOMEDICAL INSTRUMENTATION VL435	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Model biological systems.
CO2	Comprehend the principles of transducers in bio-instrumentation
CO3	Analyze the ECG, EEG and EMG
CO4	Measure bio medical signal parameters.
CO5	Study pace makers, defibrillators, surgical instruments etc.

2. Syllabus:

ANATOMY AND PHYSIOLOGY **(06 Hours)**

Elementary Ideas of Cell Structure, Heart and Circulatory System, Control Nervous System, Musclo-Skeletal System, Respiratory System Body Temperature and Reproduction System.

CLASSIFICATION OF BIOMEDICAL EQUIPMENT **(02 Hours)**

Diagnostic, Therapeutic and Clinical Laboratory Equipment.

BIOELECTRIC SIGNALS AND THEIR RECORDING **(09 Hours)**

Bioelectric Signals (ECG, EMG, ECG, EOG & ERG) and Their Characteristics, Bio- Electrodes, Electrodes Tissue Interface, Contact Impedance, Effects of High Contact Impedance, Types of Electrodes, Electrodes for ECG, EEG and EMG.

TRANSDUCERS FOR BIOMEDICAL APPLICATION **(10 Hours)**

Resistive Transducers - Muscle Force and Stress (Strain Gauge), Spirometry, Humidity, (Gamstrers), Respiration (Thermistor), Inductive Transducers: Flow Measurements, Muscle Movement (LVDT), Capacitive Transducers: Heart Sound Measurement, Pulse Pick Up, Photoelectric Transducers, Pulse Transducers, Blood Pressure, Oxygen Analyses Piezoelectric Transducers: Pulse Pickup, Ultrasonic Blood Flowmeter, Chemcial Transducer: Ag-Agfallas (Electrodes, PH Electrode).

BIOLDECTRIC SIGNAL RECORDING MACHINES **(06 Hours)**

Physiological Pre-Amplifier and Specialized Amplifiers, ECG Lead Systems Details of ECG, EMG and EEG Machines.

PATIENT MONITORING SYSTEM **(05 Hours)**

Heart Rate Measurement, Pulse Rate Measurement, Respiration, Rate Measurement, Blood Pressure Measurement, Microprocessor Applications in Patient Monitoring.

DEFIBRILLATORS AND PACEMAKERS **(05 Hours)**

Rationale of using Defibrillators, Theory of Defibrillators Circuits, Types of Defibrillators, Safety issues in Defibrillators, Theory of Pacemakers, Types of Pacemakers, Pacemaker Circuit, Technical Specification of Pacemaker, Defibrillator and Pacemaker Simulators.

SAFETY ASPECT OF MEDICAL **(02 Hours)**

Gross Current, Micro Current Shock, Safety Standards Rays and Considerations, Safety Testing Instruments, Biological Effects of X-Rays and Precautions.

	(Total Contact Hours: 45)
3.	**<u>Books Recommended:</u>**
	1. John. G. Webster, "Medical Instrumentation", John Wiley, 4th Ed., 2009 2. Amit J. Nimunkar, John G. Webster, John William Clark, “Medical Instrumentation Application and Design”, Wiley, 2020. 3. Goddes L. A. and Baker L. E., "Principles of Applied Biomedical Instrumentation", John Wiley, 3rd Ed., 1989. 4. Carr Joseph J. and Brown John M, "Biomedical Instrumentation and Measurement", Pearson, 4th Ed., 2001. 5. Cromwell, "Biomedical Instrument", Prentice Hall, 3rd Ed., 2000. 6. R.S. Khandpur,"Hand book of Medical Instruments", TMH, 2nd Ed., 2003.

B.Tech. IV (VL) Semester VII SOC DESIGN EC437	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Design and optimize a modern System-on-a-Chip
CO2	Implement both hardware and software solutions, formulate hardware/software trade-offs, and perform hardware/software codesign
CO3	Understand and estimate key design metrics and requirements including area, latency, throughput, energy, power.
CO4	Have basic exposure to SystemC programming and HLS
CO5	Appreciate issues in system-on-chip design associated with Interconnection Structures, performance and power consumption

2. Syllabus:

SOC DESIGN APPROACH **(08 Hours)**

Basics of Chips and SoC ICs, SoC Design: SoC CPU/IP Cores; Co-processor; Cache; DRAM Controller, SoC Synthesis, Static Timing Analysis (STA), Design for Testability, Verification, Physical Design,

HARDWARE-SOFTWARE CO-SYNTHESIS **(08 Hours)**

Partitioning, Cycle Time, Die Area-and-Cost, Power, Area-time-Power Trade-offs and Chip Reliability, Real-time scheduling, hardware acceleration

VIRTUAL PROTOTYPING AND HLS **(11 Hours)**

Mapping High-Level Language Applications to Hardware, Transaction-Level Modeling & Electronic System-Level Languages, Hardware Accelerators, Media Instructions, Co-processors, System-Level Design Methodology, High-Level Synthesis (C-to-RTL), Hardware Synthesis and Architecture Techniques, Source-Level Optimizations

SOC INTERCONNECTION STRUCTURES **(10 Hours)**

Bus-based Interconnection, Bus protocols: AMBA AXI Bus; AXI4-Stream; IBM Core Connect; Avalon, Interconnection Structures, Network on Chip - NoC Interconnection and NoC Systems, IP interfacing

PERFORMANCE / POWER ANALYSIS OF SOCS **(08 Hours)**

System-level modeling and integration, Simulation platform for performance analysis of SoC/MPSoC, Use cases and examples.

(Total Contact Time: 45 Hours)

3. Books Recommended:

1. Veena Chakravarthi, “A Practical Approach to VLSI System on Chip (SoC) Design-A Comprehensive Guide”, Springer, 2020
2. S. Pascricha and N. Dutt, “On-Chip Communication Architectures, System on Chip Interconnect”, Morgan Kaufmann-Elsevier Publishers, 2008.
3. Keating, M., “The Simple art of SoC design”, Springer, 2011.
4. P. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer, 2009.
5. Grotker, T., Liao, S., Martin, G. & Swan, S., “System design with SystemC”, Springer, 2002

4.	**Reference Books:**
	1. Ghenassia, F., “Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems”, Springer, 2010 2. Henry Chang, L.R. Cooke, Merrill Hunt, Grant Martin, Andrew McNelly, Lee Todd, “Surviving the SOC Revolution - A Guide to Platform-Based Design”, Springer, 1999. 3. Grant Martin, Brian Bailey, Andrew Piziali, “ESL Design and Verification: A Prescription for Electronic System Level Methodology (Systems on Silicon Series)”, Morgan Kaufmann, 2007

B. Tech. IV (VL) Semester – VII CMOS RF IC DESIGN EC 439	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Select a transceiver specification appropriate for the communication link.
CO2	Demonstrate Analog and Digital Modulation for RF circuits.
CO3	Analyze the Low Noise Amplifier (LNA).
CO4	Evaluate the appropriate mixers and oscillators for the desired applications.
CO5	Design of PLL using appropriate loop filter, phase detector and frequency synthesizer.

2. Syllabus

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: (08 Hours)

Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, inter-symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion, S-parameters with Smith chart, Passive IC components.

POWER AMPLIFIERS AND MATCHING NETWORKS (06 Hours)

Class A, AB, B and C Power amplifiers, modulation and characteristics of power amplifiers, Design examples. Impedance transformations and matching; L-matches, Pi- & T-matches, tapped-capacitor match.

LOW NOISE AMPLIFIERS (12 Hours)

LNA Topologies: Common-Source Stage with Resistive Feedback, Common Gate, Cascode CS Stage with Inductive Degeneration, Variants of Common-Gate LNA, Noise-Cancelling LNAs, Reactance-Cancelling LNAs Gain Switching, Band Switching, Differential LNAs, Nonlinearity Calculation

MIXERS AND OSCILLATORS (11 Hours)

Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature and single-sideband generators

PLL AND FREQUENCY SYNTHESIZERS (08 Hours)

Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters, Some discussion on available CAD tools for RF VLSI design

Total Contact Time: = 45 Hours

3. Books Recommended

1. T. H. Lee, “The Design of CMOS RF Integrated Circuits”, Cambridge, 2012.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2013.
3. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.
4. C.C. Enz and E.A. Vittoz, Charge-based MOS transistor Modelling The EKV Model for Low- Power and RF IC Design By, Wiley, 2006
5. Christopher Bowick, “RF Circuit Design”, Newnes, 2007

B. Tech. IV (VL) Semester – VII ANALOG MIXED SIGNAL IC DESIGN EC 441	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand sample and hold circuits based on CMOS and BiCMOS. Compare and contrast various S/H circuits.
CO2	Apply advanced techniques for bandgap references, comparators, current mirrors and operational amplifiers.
CO3	Evaluate concepts of Oversampled ADCs, Noise shaping and decimation filtering. Propose and design sigma-delta architecture based on specification
CO4	Analyze a variety of data converters. Compare architectures based on various metrics.
CO5	Design of various mixed signal blocks

2. Syllabus

SAMPLE AND HOLD CIRCUITS **(8 Hours)**

Sample & hold and trans-linear circuits - performance and testing of sample and hold circuits, examples of CMOS S/H circuits, bipolar and BiCMOS S/H circuits, trans-linear gain cell and multipliers. Switched capacitor circuits – op-amps, capacitors, switches, non-overlapping clocks

SWITCHED CAPACITOR CIRCUITS **(6 Hours)**

Basic operation and analysis of switched capacitor circuits, resistor equivalence of a switched capacitor, noise in switched-capacitor circuits. Comparators - specifications, op-amp as a comparator, latched comparators, examples of CMOS comparators

A TO D AND D TO A CONVERTERS **(12 Hours)**

Data convertors - ideal D/A and A/D convertors, quantization noise, accuracy and linearity. Nyquist rate DAC - Decoder-based converter, Binary-scaled converters, Thermometer-code converters, Hybrid converters. Nyquist rate ADC - Successive-approximation converters, Algorithmic (or cyclic) A/D Converter, Pipelined A/D converters, Two-step A/D converters, Interpolating A/D converters, folding A/D converters, time-interleaved A/D converters

OVERSAMPLED DATA CONVERTERS **(12 Hours)**

Oversampling ADCs - Oversampling without noise shaping - quantization noise modeling, white noise assumption, • oversampling advantage, the advantage of 1-bit D/A converters. Oversampling with noise shaping - noise-shaped delta-sigma modulator, first-order noise shaping, switched-capacitor realization of a first-order A/D converter, quantization noise power of 1-bit modulators. System architectures, Digital decimation filters, Multi-bit oversampling converters

MIXED SIGNAL SUBCIRCUITS **(7 Hours)**

Linearized PLL models, Design of PLL's and DLL's and frequency synthesizers, VCO, Jitter and phase noise, Electronic oscillators

Total Contact Time: = 45 Hours

3.	**Books Recommended**
	1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, “Analog Integrated Circuit Design”, 2nd Edition, John Wiely & Sons, 2012. 2. B. Razavi, “Principles of Data Conversion System Design”, 1st Edition, Wiley-IEEE Press, 1994 3. R. J. Baker, “CMOS Mixed Signal circuit Design”, 2nd Edition, Wiley 2008 4. M.Gustavsson, J. J. Wikner, and N. N. Tan, "CMOS Data Conversion for Communications", Kluwer 2000. 5. Emad N. Farad and Mohamed I. Elmasry, “Mixed Signal VLSI Wireless Design: Circuits and Systems”, Kluwer 2002

B.Tech. IV (VL) Semester VII HARDWARE ARCHITECTURES FOR DEEP LEARNING VL443	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe approximate data representation and its significance for deep learning
CO2	Discuss model sparsity for dense accelerator
CO3	Discover the usage of various computation support for hardware architecture
CO4	Analyze the embedded system implementation of convolution neural network.
CO5	Design iterative CNN solution for low power and real-time systems

2. Syllabus:

DEEP LEARNING AND APPROXIMATE DATA REPRESENTATION (08 Hours)

Introduction – Background, Stochastic computing, Deterministic low-discrepancy bit-streams,Convolutional neural networks, Convolutional neural networks, Related work, Proposed hybrid binary-bit-stream design, Multiplications and accumulation, Handling negative weights,Experimental results, Performance comparison, Cost comparison, Binary neural networks, Binary and ternary weights for neural networks, Binarized and ternarized neural networks,NN optimization techniques, Hardware implementation of BNNs

DEEP LEARNING AND MODEL SPARSITY (10 Hours)

Different types of sparsity methods, Software approach for pruning, Hard pruning, Soft pruning, structural sparsity, and hardware concern, Questioning pruning, Hardware support for sparsity, Advantages of sparsity for dense accelerator, Supporting activation sparsity, Supporting weight sparsity, Supporting both weight and activation sparsity, Efficient inference engine

COMPUTATION REUSE-AWARE ACCELERATOR FOR NEURAL NETWORKS (07 Hours)

Baseline architecture, Computation reuse support for weight redundancy, Computation reuse support for input redundancy, Multicore neural network implementation – More than K weights per neuron, More than N neurons per layer

CONVOLUTIONAL NEURAL NETWORKS FOR EMBEDDED SYSTEMS (10 Hours)

Brief review of efforts on FPGA-based acceleration of CNNs, Network structures and operations – Convolution, Inner product – Pooling, Other operations, Optimizing parallelism sources,Identifying independent computations, Acceleration strategies, Computation optimization and reuse, Design control variables, Partial sums and data reuse, IFMs first strategy, OFMs first strategy, Proposed loop coalescing for flexibility with high efficiency, Bandwidth matching and compute model, Resource utilization, Unifying off-chip and on-chip memory, Impact of unmatched system, Effective bandwidth latency, Analyzing runtime, Estimating required offchip bandwidth, Library design and architecture implementation, Concurrent architecture, Convolution engine, Optimal DRAM access, Restructuring fully connected layers – Zero overhead pooling, Other layers, Caffe integration, Performance evaluation, Optimizer results, Latency estimation model, Exploration strategy, Design variable optimization, Onboard runs, Network-specific runs, Cross-network run, Architecture comparison, Raw performance improvement.

ITERATIVE CONVOLUTIONAL NEURAL NETWORK (ICNN): AN ITERATIVE CNN SOLUTION FOR LOW POWER AND REAL-TIME SYSTEMS (10 Hours)

Optimization of CNN, Iterative learning, Case study: iterative AlexNet, ICNN training schemes, Sequential training, Parallel training, Complexity analysis – Visualization, Background on CNN visualization, Visualizing features learned by ICNN, Contextual awareness in ICNN, Prediction rank,

	Pruning neurons in FC layers, Pruning filters in CONV layers, Policies for exploiting energy-accuracy trade-off in ICNN, Dynamic deadline (DD) policy for real-time applications, Thresholding policy (TP) for dynamic complexity reduction, Fixed thresholding policy – Context-aware pruning policy, Context-aware pruning policy for FC layer – Context aware pruning policy for CONV layer
	(Total Contact Time: 45 Hours)
3.	**Books Recommended:**
	1. Masoud Daneshtalab and Mehdi Modarressi, "Hardware Architectures for Deep Learning (Materials, Circuits and Devices)", IET Publications, 2020. 2. Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel S. Emer, "Efficient Processing of Deep Neural Networks", Springer Nature, 31 May 2022 3. Bert Moons, Daniel Bankman, and Marian Verhelst, "Embedded Deep Learning Algorithms, Architectures and Circuits for Always-on Neural Network Processing", Springer International Publishing ,2018. 4. Albert Chun-Chen Liu, Oscar Ming Kin Law, "Artificial Intelligence Hardware Design Challenges and Solutions", Wiley Publication, 2021 5. Brandon Reagen, Robert Adolf, Paul Whatmough, Gu-Yeon Wei, David Brooks, and Margaret Martonosi, "Deep Learning for Computer Architects (Synthesis Lectures on Computer Architecture)", Morgan and Claypool Life Sciences,2017.
4.	**Reference Books:**
	1. V. Sze, "Designing Hardware for Machine Learning," in IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 46-54, Fall 2017. 2. Mingu Kang, Sujan Gonugondla, Naresh R. Shanbhag", Deep In-memory Architectures for Machine Learning", Springer International Publishing, 2020

B.Tech. IV (VL) Semester VII ERROR CORRECTING CODING EC427	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Understand channel coding theorem , importance of error correction in data communication
CO2	Discuss various mathematical tools: groups and finite fields, Linear algebra in the development of codes and sequences.
CO3	Analyze various Block code encoder and decoder
CO4	Design and Develop different error correcting codes for appraise of reaching data rate to Shannon limit.
CO5	Compare and contrast the strengths and weaknesses of various errors correcting code

2. Syllabus:

CHANNEL CAPACITY AND CODING **(05 Hours)**

Introduction, Communication system block Diagram, Channel Models, Channel Capacity, Channel Coding, The Shannon Limit, Hamming Distance, Channel code rate, Few Points of Information Theory. Decoding Probability

BLOCK CODES **(05 Hours)**

Introduction to Block Codes, Single Parity Check Codes, Product Codes, Repetition Codes, Hamming Codes, Minimum Distance Of Block Codes, Soft - Decision Decoding, Automatic Repeat Request Schemes.

LINEAR CODES **(06 Hours)**

Definition of Linear Codes, Generator Matrices, The Standard Array, Parity - Check Matrices, Error Syndromes, Error Detection And Correction, Shortened And Extended Linear Codes.

CYCLIC CODES **(06 Hours)**

Definition Of Cyclic Codes, Polynomials, Generator Polynomials, Encoding Cyclic Codes, Decoding Cyclic Codes, Factors Of xn+1, Parity-Check Polynomials, Dual Cyclic Codes, Generator And Parity-Check Matrices Of Cyclic Codes, Design of cyclic Encoder using LFSR, Cyclic Decoder using LFSR, The Meggitt Decoder

BCH CODES **(10 Hours)**

Linear Algebra, Galois Field, Primitive Field elements, Irreducible and primitive polynomials, minimal polynomials, Definition and Construction of Binary BCH Codes, Error Syndromes In Finite Fields, Decoding SEC and DEC Binary BCH codes, The Error location Polynomial, the Peterson Gorenstein Zierler decoder, Reed-Solomon Codes

CONVOLUTION CODES **(08 Hours)**

Convolution, Encoding Convolutional Codes, Generator Matrices for Convolutional Codes, Generator Polynomials For Convolutional Codes, Graphical Representation Of Convolutional Codes, The Viterbi Decoder

ADVANCE ERROR CONTROL CODING **(05 Hours)**

Concept Of Puncturing, Interlever, Turbocode, Introduction to LDPC Codes, Applications of Error Control Coding

(Total Contact Time: 45 Hours)

3.	**Books Recommended:**
	1. Gravano Salvatore, "Introduction to Error Control Codes", 1st Ed., Oxford University Press, 2007. 2. Shu Lin/ Daniel J. Costello Jr., "Error Control Coding, Fundamental and Applications, Prentice Hall series in computer applications in electrical engineering" 2nd Ed., Series, 2005. 3. Ranjan Bose, "Information theory, coding and cryptography", Tata McGraw-Hill,2nd Edition, April 2008 4. Moon Tood K., "Error Correction Coding - Mathematical Methods and Algorithms", 1st Ed., Wiley- Interscience, 2006. 5. Sklar Bernard, "Digital Communications - Fundamentals and Applications", 2nd Ed., Pearson Education-LPE, 2009

B.Tech. IV (VL) Semester VII DEEP LEARNING EC435	Scheme	L	T	P	Credit
		3	0	0	03

1. Course Outcomes (COs):

At the end of the course the students will be able to:

CO1	Describe Basic Concepts of Machine Learning, Pattern Classification, and Neural Network (NN), and Explain How NN Learn and Function.
CO2	Demonstrate and Implement Single-Layer and Multi-Layer Perceptron Learning Algorithms, Analyzing Their Effectiveness for Various Classification Tasks.
CO3	Examine The Principles of Deep Learning Algorithms, Including CNNs And RNNs, and Apply Them to Various Applications Like Image and Sequence Data Processing.
CO4	Evaluate the Performance of Deep Learning Models Using Different Optimization Techniques and Network Training Strategies.
CO5	Design and Develop Advanced Deep Learning Models, Utilizing Principles of Regularization and Optimization, for Real-World Applications in Different Domains.

2. Syllabus:

INTRODUCTION **(07 Hours)**

Brief History and Evaluation of Deep Learning, Brief Overview of Supervised and Unsupervised Machine Learning Algorithms, Difference Between Machine Learning and Deep Learning, Applications of Deep Learning, Review of Linear Algebra, Vector Calculus and Probability Theory, Discriminant Function and Decision Surface, Perceptron Algorithm.

INTRODUCTION NEURAL NETWORKS **(12 Hours)**

Biological Inspirations for Artificial Neurons, Single Layer Perceptron, Multilayer Perceptron (MLP), Activation Functions, Loss Functions, Computational Graph, Back Propagation Algorithm, Example of Back Propagation, Vanishing and Exploding Gradient Problem, Overfitting and Underfitting, Bias-Variance Trade-off, Autoencoder, Autoencoder vs PCA.

CONVOLUTIONAL NEURAL NETWORK (CNN) **(08 Hours)**

Convolution, Cross Correlation, Padding, Stride, Pooling, and Their Impact on the Output Dimension, Receptive Filed and Feature Maps, Building Blocks of CNN, MLP vs CNN, Popular CNN architectures: LeNet, AlexNet, VGG, ResNet, GoogleNet, Transfer Learning, Modern CNN Architectures.

OPTIMIZATION TECHNIQUES AND REGULARIZATION **(06 Hours)**

Gradient Descent (GD), Batch GD, Mini-Batch GD, Stochastic GD, Momentum Optimizer, Momentum and Nesterov Accelerated Gradient (NAG) Optimizer, RMSProp, Adam. Regularization Techniques: L1, L2 Regularization, Dropout, Early Stopping. Batch Normalization, Instance Normalization, Group Normalization.

SEQUENTIAL AND GENERATIVE MODELS **(12 Hours)**

Basics of Sequence Data and Recurrent Neural Network (RNN) Architecture, Long Short-Term Memory (LSTM), Challenges in Training RNNs (Exploding/Vanishing Gradients), Word Embedding, Attention Mechanism, Transformer Architecture, Comparison Between RNNs, CNNs, and Transformers, Overview of Generative Models, Difference Between Generative and Discriminative Models, Variational Autoencoders, Generative Adversarial Networks, Recent Trends in Deep Learning.

(Total Contact Hours: 45)

3.	**List of Practicals:**	
	1. Introduction to Python for machine learning. 2. To learn data handling, visualization and pre-processing in Python. 3. Implement multilayer perceptron using back propagation for classification. 4. Implement and compare various optimization techniques (RMSprop, Adam, Adagrad) 5. Implement principal component analysis (PCA) and Autoencoder for dimensionality reduction and compare their performance. 6. Implement Autoencoder for image denoising. 7. Implement CNN for binary and multiclass classification and adjust hyper parameters to improve the classification accuracy. 8. Perform Image Segmentation using Deep Learning Models. 9. Implement recurrent neural network for time series prediction. 10. Implement LSTM for time series prediction and compare its performance with RNN. 11. Implement Attention Based Model for Machine Translation. 12. Implement GAN for Image Generation.	
4.	**Books Recommended:**	
	1. Ian Goodfellow, Yoshua Benjio, Aaron Courville, "Deep Learning," 1st Ed, The MIT Press, 2017. 2. Eugene Charniak, "Introduction to Deep Learning," 1st Ed, The MIT Press, 2019. 3. Charu C. Aggarwal, "Neural Networks and Deep Learning: A Textbook," 1st Ed, Springer, 2018. 4. Francois Chollet, "Deep Learning with Python," 1st Ed, Manning, 2017. 5. David Foster, "Generative Deep Learning: Teaching Machines to Paint, Write, Compose, and Play," 1st Ed, O'Reilly Media, 2022.	
5.	**Reference Book and Materials:**	
	1. Christopher M. Bishop, "Pattern Recognition and Machine Learning", Springer; 2nd Ed., 2011. 2. Aurélien Géron, "Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems," 3rd Ed, O'Reilly Media, 2022.	