डिपार्टमेंट ऑफ़ इलेक्ट्रॉनिक्स इंजीनियरिंग
DEPARTMENT OF ELECTRONICS ENGINEERING
सरदार वल्लभभाई नेशनल इंस्टिट्यूट ऑफ़ टेक्नोलॉजी, सूरत
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT

क्रमांक:**DECE/ISRO/2042/ 2024-25** दिनांक:**10/01/2025**

Recruitment of Project Staff on Purely Contract Basis

Applications are invited on prescribed format for the post of Junior Research Fellow on purely contract basis for one year (may be extended further) for ISRO Sponsored Research Project entitled "Onboard spectral preprocessing for multispectral image compression using FPGA" at the institute. The application form and the details of all educational qualifications and relevant experience required for various positions are available on Institute website http://www.svnit.ac.in**.** Duly filled and signed application form along with self-attested scanned M. Tech. / Ph. D. mark-sheets of all semesters, relevant experience certificates and necessary documents must be submitted in a single PDF file by email at add@eced.svnit.ac.in on or before **20h January, 2025** with subject "**Application for the post of JRF**".

Sr. No	Post	Qualification	Experience	No. of. Posts / Duration	Consolidated Pay (Per Month)
1.	Junior Research Fellow	B. E. / B. Tech. (Electronics / Electronics & Communication) **OR** M.E / M. Tech in VLSI Design / Microelectronics / Microelectronics and VLSI Design / M. Sc. Electronics / Physics Selected through a process described any one of the following: a. Scholar who are selected through National Eligibility Tests –JEE, CSIR – UGC NET including lectureship (Assistant Professorship) and GATE b. The Selection process through National level examinations conducted by Central Government Departments and their agencies and Institutions such as DST / DBT / DAE / DOS / DRDO / MoE / ICAR / ICMR / IIT / IISc. /IISER /NISER etc.	**Knowledge of Image Processing Algorithms, Digital Signal Processing, Karhunen-Loève (KL) Transform and Pairwise orthogonal transform for spectral image coding, Consultative Committee for Space Data Systems (CCSDS) standards, FPGA Design flow, Verilog/VHDL** **Software Skills: Xilinx Vivado, MATLAB, C/C++**	1 Post/ till March, 2025 and Extendible till project duration	Rs. 37,000/- p.m. + 18% HRA

Note:

1. The above positions are purely contractual for 1 Year and can be extended till project duration based on the performance evaluation every year.
2. The last date for receiving applications is **20th January, 2025.**
3. Institute will not be responsible for any postal delay.
4. Applications received after last date will not be considered.
5. The list of shortlisted candidates will be displayed on the institute website on **22nd January, 2025**.
6. Interview/Test for the shortlisted candidates will be held on **24th January, 2025.** However, ***final date/venue of Interview/Tests will be communicated in the intimation email.***
7. An applicant has to ensure the authenticity of information provided in support of experience claimed, other documents and photograph.
8. The qualification and experience may be relaxed at any point of time by the Institute for otherwise exceptional candidates.
9. **Request for the online Interview will be considered.**
10. **No TA/DA will be paid for appearing in the Interview**.
11. Candidate employed in institute/Industry must produce No-Objection Certificate (NOC) at the time of interview.
12. List of selected candidates will be displayed on the institute website within one week after interview held.
13. Candidates who got selected may be allowed to enroll for Ph.D. program subject to the fulfillment of eligibility conditions of SVNIT, Surat.

DIRECTOR
SVNIT, Surat

DEPARTMENT OF ELECTRONICS ENGINEERING
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ICHCHHANATH, SURAT-395007 (GUJARAT)
website: www.svnit.ac.in

APPLICATION FORM

1.	Post applied for		Self Attested Photograph
2.	Name of the Candidate		
3.	Address of the Candidate		
4.	Father's Name		
5.	Date of Birth		
6.	Age as on last date of application	_____Years _____ Months _____ Days	
7.	Contact No. (Mobile)		
8.	Email Id.		

9. Educational Qualification (Photocopy of certificate/degree must be attached)

Qualification	**Subject/Discipline**	**Board/Institute /University**	**Year**	**% of marks/ CGPA obtained (Aggregate)**
10th or equivalent				
12th or equivalent				
Bachelor Degree				
Master Degree				
Ph.D.				
Master Degree Thesis Title				
Ph.D. Thesis Title				

8. Relevant Experience (Details of Employment in chronological order. Enclose a separate sheet duly authenticated under your signature if necessary)

Organization	**Post Held**	**From**	**To**	**Pay Drawn**	**Nature of Duties**

9.	**Total emoluments per month presently drawn.**	
10.	**Additional information if any, which you would like to mention in support of your suitability for the post, (attached separate sheet if necessary)**	

Declaration

I hereby declare that the information furnished above is true to the best of my knowledge and belief. If at any time it is found that I have concealed any information or have given any incorrect data, my candidature/appointment, may be cancelled/terminated, without any notice or compensation.

Place:
Date:

Signature of the Candidate