DEPARTMENT OF ELECTRONICS ENGINEERING
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT

क्रमांक:**DECE/ISRO/ 4091 / 2024-25** दिनांक:**10/02/2025**

Recruitment of Project Staff on Purely Contract Basis

Applications are invited on prescribed format for the post of Junior Research Fellow on purely contract basis for one year (may be extended further) for ISRO Sponsored Research Project entitled "Onboard spectral preprocessing for multispectral image compression using FPGA" at the institute. The application form and the details of all educational qualifications and relevant experience required for various positions are available on Institute website http://www.svnit.ac.in**.** Duly filled and signed application form along with self-attested scanned M. Tech. / Ph. D. mark-sheets of all semesters, relevant experience certificates and necessary documents must be submitted in a single PDF file by email at add@eced.svnit.ac.in on or before **24th February, 2025** with subject "**Application for the post of JRF / Project Associate**".

Eligibility Criterion:

For Sr. No. 1: As per OM DST/PCPM/Z-06/2022 dtd. 26/06/2023

For Sr. No. 2 and 3: as per DST OM SR/S9/Z-05/2019 dtd. 10/07/2020.

Sr. No	Post	Qualification	No. of. Posts / Duration	Desired Skills	Salary
1.	Research Personnel (Junior Research Fellow)	B. E./ B.Tech./ M. E. / M. Tech in VLSI Design / Microelectronics / Microelectronics and VLSI Design / M. Sc. Electronics / Electronics & Communication / or equivalent **Qualified in National Level eligibility test CSIR-UGC NET/ GATE**	01 Post/ 2½ Months and extendible on yearly review-basis till the duration of the project.	Knowledge of Image Processing Algorithms, Digital Signal Processing, Karhunen-Loève (KL) Transform and Pairwise orthogonal transform for spectral image coding, Consultative Committee for Space Data Systems (CCSDS) standards, FPGA Design flow, Verilog/VHDL Software Skills: Xilinx Vivado, MATLAB, C/C++	Rs. 37,000/- + HRA@ 18% p.m.
Note: The candidate shall note that this Advt. is for 1 POST of JRF / Project Associate. The post will be filled for Research Personnel (JRF). However, in case of non-availability of suitable candidates for the post of Research Personnel (JRF), or in case Non receipt of any application meeting the qualification norms mentioned for JRF, the recruitment of Research Personnel (Project Associate) will be considered. The eligibility criterion for the said post of Research Personnel (Senior Project Associate/Project Associate) is mentioned below.					
2.	Research Personnel (Project Associate)	B. E./ B.Tech./ M.E / M. Tech in VLSI Design / Microelectronics / Microelectronics and VLSI Design / Electronics & Communication / M. Sc. Electronics or equivalent **Upper Age Limit:** 35 years	01 Post/ 2½ Months and extendible on yearly review-basis till the duration of the project.	Knowledge of Image Processing Algorithms, Digital Signal Processing, Karhunen-Loève (KL) Transform and Pairwise orthogonal transform for spectral image coding, Consultative Committee for Space Data Systems (CCSDS) standards, FPGA Design flow, Verilog/VHDL Software Skills: Xilinx Vivado, MATLAB, C/C++	Rs. 25,000/- + HRA@ 18% p.m.

Note:

1. The above positions are purely contractual for 2½ months and can be extended till project duration based on the performance evaluation every year.
2. The last date for receiving applications is **24th February, 2025.**
3. Applications received after last date will not be considered.
4. The list of shortlisted candidates will be displayed on the institute website on **25th February, 2025**.
5. Interview/Test for the shortlisted candidates will be held on **28th February, 2025.** However, ***final date/venue of Interview/Tests will be communicated in the intimation email.***
6. **Request for the online Interview will be considered. No TA/DA will be paid for appearing in the Interview**.
7. Candidate employed in institute/Industry must produce No-Objection Certificate (NOC) at the time of interview.
8. List of selected candidates will be displayed on the institute website within one week after interview held.
9. Candidates who got selected may be allowed to enroll for Ph.D. program subject to the fulfillment of eligibility conditions of SVNIT, Surat.

REGISTRAR
SVNIT, Surat