Date: 30/07/2024

Advertisement for Research Personnel in the SERB-DST Sponsored Project

Applications are invited from eligible candidates for the position of Research Personnel (JRF / Senior Project Associate) in a sponsored research project funded by the Science and engineering research board (SERB), Ministry of Science and Technology, Government of India, under the supervision of Dr. Abhishek Acharya. The duration of the position is a maximum of three years. The selected candidate may have the opportunity to register in the Ph.D. program as per institute norms. The details of the project are mentioned below:

Title of the project	**Design and Characterization of Radiation Hardened Standard Cell Library using Nanosheet Field Effect Transistors: Improving on Design Margins/Reliability**
Name & address of sponsoring agency	Science and Engineering Research Board (SERB), DST, Govt. of India, New Delhi
Research Personnel	Junior Research Fellow/ Senior Project Associate
No. of post	01
Duration	One year, extendable till the project ends
Principal Investigator	Dr. Abhishek Acharya, Department of Electronics Engineering, Sardar Valllabhbhai National Institute of Technology Surat-395007 (Gujarat)
Essential Qualification	**Junior Research Fellow** First Class M.E. / M.Tech. or B.E. / B.Tech. in Microelectronics & VLSI, VLSI & Embedded Systems, Electronics Engineering, Electronics & Communication Engineering, or related Allied branches selected through a process describing though any of the following: a) Scholars who are selected through National Eligibility Test – CSIR UGC NET and GATE b) The selection process through National Level Examinations conducted by Central Govt. Department and their agencies. The qualification and criterion of selection for JRF is as per OM No. DST/PCPM/Z-06/2022, dated 26/06/2023, please refer the same for more details. **OR** **Senior Project Associate** First Class M.E. /M.Tech. or B.E./B.Tech. in Microelectronics & VLSI, VLSI & Embedded Systems, Electronics Engineering, Electronics & Communication Engineering, or related Allied branches with four years of experience in research and development in industrial and academic institution or science and technology organization and scientific activities and services. The qualification and criterion of selection for Senior Project Associate is as per OM No. SB/S9/Z-07/2020, dated 25/08/2020, please refer the same for more details.
Desirable Qualification	Background in Microelectronics & VLSI Design, knowledge of EDA Tools, Linux platform
Fellowship	Rs. 37000/- per month for JRF **OR** Rs. 42000/- per month for Senior Project Associate
How to apply	A soft copy of the scanned application form with supporting documents may be sent via email abhishek@eced.svnit.ac.in on or before 15-08-2024. Original documents, including age proof, certificates, degrees, mark sheets, and other testimonials, must be presented at the time of the interview. Date of National Level Test/Interview: will be communicated through email / institute website).
Address of Correspondence	Abhishek Acharya, Associate Professor Department of Electronics Engineering, Sardar Vallabhbhai National Institute of Technology Surat Ichchhanath, Dumas Road - 395007, Gujarat, India

Interested candidates are required to note the following:

1. The interested candidates will be required to submit their application form along with all essential details and scanned copy of all their original certificates, mark sheets and a recent passport size photograph by the last date, *i.e*, 15/08/2024, 05:00 PM. Clearly state the post applied for (JRF/SRF/Senior Project Associate) in the application form (Annexure 1).
2. Candidates need to bring the complete hardcopy set of the application form with xerox copies of all required documents on the day of interview for verification purpose.
3. Candidates are required to positively mention their e-mail ID and Mobile Number in the Application Form.
4. The applications received within the last date & time stipulated will be screened by a selection committee, and a list of eligible candidates shortlisted for National Level test / Interview will be communicated through email / institute website. The Screening Committee may devise its own criteria for shortlisting of candidates for interview as per OM No. DST/PCPM/Z-06/2022, dated 26/06/2023 and SB/S9/Z-07/2020, dated 25/08/2020.
5. The decision of SVNIT-Surat in all matters relating to eligibility, acceptance, screening, mode of selection will be final and binding on the candidates and no enquiry correspondence will be entertained in this connection from any individual or any agency on behalf of the candidate.
6. The original documents of selected candidates will be verified at the time of Interview, and in the event of any information mentioned in application/CV/testimonials found false or incorrect, their candidature straightway shall be cancelled.
7. No TA/DA will be paid for attending the interview/test.
8. For any queries regarding the position, please email Dr. Abhishek Acharya at abhishek@eced.svnit.ac.in.

Director