DEPARTMENT OF ELECTRONICS ENGINEERING
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ICHCHHANATH, SURAT-395007 (GUJARAT)
website: www.svnit.ac.in

Ref No.

Date: February 27, 2021

**Recruitment of Project Staff on Purely Contract Basis**

Applications are invited on prescribed format for the post of Guest Faculty and Lab Engineer on purely contract basis for one year (may be extended further) for MeitY, Government of India, New Delhi sponsored project entitled "Special Manpower Development Programme for Chips to System Design" at the institute. The application form and the details of all educational qualifications and relevant experience required for various positions are available on Institute website http://www.svnit.ac.in. Duly filled and signed application form along with self-attested scanned M. Tech. / Ph. D. mark-sheets of all semesters, relevant experience certificates and necessary documents must be submitted in a single PDF file to **"Chief Investigator, SMDP - C2SD Project, Department of Electronics Engineering, S. V. National Institute of Technology, Surat, Gujarat – 395007"** on or before **15th March, 2021** by email at c2sdsvnit@gmail.com. Applications received after said date will be not considered.

**(Dr. A. D. Darji)**
**CI, SMDP - C2SD Project**
**SVNIT Surat**

**Eligibility Criterion:**

| Sr. No | Post | Qualification | Experience | No. of. Posts / Duration | Consolidated Pay (Per Month) |
|---|---|---|---|---|---|
| 1. | Guest faculty | M.E/M. Tech* in VLSI / Microelectronics / Embedded system with minimum 3 years research & development experiences<br>OR<br>Ph.D. with specialisation in VLSI Design/ Embedded Design/ System Design. | • Carrying out R & D work in VLSI Design related project<br>• Good knowledge of CAD Tools (such as Cadence, Synopsys, Mentor), RTL Coding, Physical Design, Chip Testing and Verification<br>• System design using Xilinx Boards | 1 Post** / 11 months (Extended up to November 2021 based on performance) | Rs. 51,245/- |
| 2. | Lab Engineer | M.E / M. Tech* in VLSI / Microelectronics / Embedded system / Design development using Xilinx Boards with minimum 2 years experiences | • Carrying out R & D work in VLSI Design related project<br>• Good knowledge of CAD Tools (such as Cadence, Synopsys, Mentor), RTL Coding, Physical Design, Chip Testing and Verification<br>• Good Knowledge of CAD Tool Management on Linux / Cent Os platform | 1 Post** / 11 months (Extended up to November 2021 based on performance) | Rs. 36,600/- |

*Aggregate First Class /CGPA 6.5 in M.E / M. Tech.
** Requirement may change at the time of interview.

**Note:**

1. Candidate having minimum aggregate First Class/CGPA 6.5 in B.E/B. Tech/M. E/M. Tech can only apply.
2. The above positions are purely contractual for one year and can be extended to five year based on the performance evaluation every year.
3. The last date for receiving applications is **15th March, 2021.**
4. Institute will not be responsible for any postal delay.
5. Applications received after last date will not be considered.
6. The list of shortlisted candidates will be displayed on the institute website on **17th March, 2021**.
7. **ONLINE** Interview/Test for the shortlisted candidates will be held on **20th March, 2021.** However, ***final date/venue of Interview/Tests will be communicated in the intimation email.***
8. An applicant has to ensure the authenticity of information provided in support of experience claimed, other documents and photograph.
9. The qualification and experience may be relaxed at any point of time by the Institute for otherwise exceptional candidates.
10. **No TA/DA will be paid for appearing in the Interview.**
11. Candidate employed in institute/Industry must produce No-Objection Certificate (NOC) at the time of interview.
12. List of selected candidates will be displayed on the institute website within one week after interview held.
13. Candidates who got selected may be allowed to enroll for Ph.D. program subject to the fulfillment of eligibility conditions of SVNIT, Surat.