SVNIT SURAT

इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते

eInfochips An Arrow Company

# CERTIFICATE COURSE ON DIGITAL IC DESIGN

## EXECUTIVE SUMMARY

**Department of Electronics Engineering, SVNIT Surat**, in collaboration with e**Infochips (An Arrow Company)**, presents a **4-month online Certificate Course** on Digital IC Design for Employability Enhancement. Tailored for **recent graduates** working in industry, undergraduate students, and faculty members, this intensive refresher course offers 60 hours of fast-paced theory and hands-on lab sessions, delivered by distinguished faculty with rich academic and industry experience. The program will serve as an excellent launchpad for a successful career in VLSI Circuits Design and ASIC Design.

## ABOUT SVNIT, SURAT

**Sardar Vallabhbhai National Institute of Technology (SVNIT)**, Surat was established in 1961 as SVRCET and became a Deemed University in 2002. It was later declared an Institute of National Importance under the NIT Act, 2007 and offering UG/PG/PhD programmes in various disciplines of Engineering, Science and Managment.

## PREFACE

The global semiconductor industry is on track to reach a trillion-dollar valuation by 2030, driving a sharp rise in demand for efficient and specialized integrated circuit (IC) design. The Advanced Certification Course on Digital IC Design by the Department of Electronics Engineering of SVNIT Surat prepares participants for careers in the semiconductor industry. Covering Digital VLSI, RTL design, Physical Design, and Processor Architecture, the program blends theory with hands-on experience using industry-standard tools. Through practical projects and case studies, learners gain the skills to tackle real-world IC design challenges.

**APPLY BEFORE : 25/06/2025**

**Limited Seats available**
**Register now to secure your future in chip design!!**

**REGISTER NOW**

https://forms.gle/57unZk6ygUdvtEyv5

## COURSE DETAILS

**Duration** : 4 Months (60+ hours)
**Start Date** : 28/06/2025
**Mode of Teaching** : Online on Weekends
**Tentative Fee** : ₹10,000/-(Including 18% GST) Students
₹20,000/-(Including 18% GST) Working Professionals

## ELIGIBILITY

- Students of B.Tech IV Year/M.Tech/ recently graduated (Year 2025) are eligible for the Student Registration Category
- Graduates from relevant fields
- Faculty members from academic institutions
- Professionals from the industry

**DATES: 28/06/2025 - 11/10/2025**

## COURSE COORDINATORS:

**Dr. Anand Darji | Dr. Zuber Patel**
**Dr. Pinal Engineer | Dr. Sandeep Mishra**
**Contact : 9316702206**
**Email : ngs_proj@eced.svnit.ac.in**

cadence AMD XILINX ChipIN IEEE SVNIT Student Branch IESA INDIA ELECTRONICS & SEMICONDUCTOR ASSOCIATION

**Chief Patron**
**Prof. Anupam Shukla**
Director,
SVNIT Surat

**Patron**
**Dr. Shilpi Gupta**
**Head, Dept. of Electronics Engg.,**
SVNIT Surat

# FACULTY OF THE PROGRAM

| Name | Designation | Area Of Expertise |
|---|---|---|
| Dr. Anand Darji | Professor, SVNIT Surat | FPGA/ASIC Design |
| Dr. Zuber M. Patel | Associate Professor, SVNIT Surat | RTL Design |
| Dr. Pinalkumar Engineer | Associate Professor, SVNIT Surat | Processor Architecture and RISC-V |
| Dr. Sandeep Mishra | Assistant Professor, SVNIT Surat | Low Power and Memory Design |
| Dr. Dipesh Panchal | Physical Design Engineer, eInfochips | Academics & Physical Design |
| Mr. Ajay Jani | Delivery Manager, eInfochips | Verification and Validation |
| Dr. Jayesh Munjani | ASIC Physical Design Engineer, eInfochips | Physical Design |
| Dr. Jignesh Patoloiya | Sr. Engineer, einfochips | Processor Architecture |
| Mr. Dhaval Fichadia | ASIC-DFT Engineer, eInfochips | SCAN-ATPG Simulation |
| Mrs. Ila Vaghela | Physical Design Engineer, eInfochips | Physical Design |
| Mrs. Ria Soni | Senior Engineer, eInfochips | Physical Design and STA |
| Dr. Priyank Prajapati | Senior Project Associate, C2S Project, SVNIT | FPGA/ASIC Digital VLSI Design |
| Mr. Niket Singla | Project Associate, C2S Project, SVNIT | Physical Design (RTL2GDS) |

## TOPICS COVERED IN THE COURSE

### Verilog HDL : RTL Design and Synthesis

- Introduction to Verilog HDL
- Data Types
- Verilog Operators
- Assignments
- Finite State Machine
- Synthesis
- Advanced Verilog for Verification

### Processor Architecture

- Introduction to Computer Architecture
- Data Path: Multipliers, MAC, Systolic Array etc
- Instruction Set Architecture (RISC V)
- Pipelining and hazards
- Memory Hierarchy
- Introduction to SoC Architecture

### Digital IC Design

- CMOS ASIC Design Flow
- CMOS Circuit Design
- Delay, Setup and Hold Time Analysis
- Combinational and Sequential Circuits
- Low-Power Design
- DFT, SCAN, ATPG
- Packaging

### Physical Design

- Overview of ASIC Design Flow
- Logic Synthesis
- Formal Verification
- Floor-Plan & Placement
- Static Timing Analysis (STA)
- Clock Tree Synthesis (CTS)
- Routing and DRC
- Layout Parasitic Extraction
- Post layout simulation
- Tapeout

### CAD Software Tools

- Circuit Simulation Tool: Spice
- Verilog RTL Design
- Simulation Tool: Xilinx Vivado
- ASIC Design:
  Cadence Genus and Innovus
- Operating System: Linux