सरदार वल्लभभाई राष्ट्रीय प्रौद्योगिकी संस्था, सुरत
सरदार वल्लभभाई राष्ट्रीय प्रौद्योगिकी संस्थान, सूरत
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
(An Institute of National Importance, Established under NITSER Act by Ministry of Education, Govt. of India)

SUCHI SEMICON

Training Programme on VLSI Design, Semiconductor Process Technology, and Packaging

Organized by

Department of Electronics Engineering
Sardar Vallabhbhai National Institute of Technology, Surat, Gujarat
In association with
Suchi Semicon

SVNIT Surat, in association with Suchi Semicon, is going to organize a training program on **VLSI Design, Semiconductor Process Technology, and Packaging** in Offline Mode. This program aims to develop specialized manpower in VLSI Design, Semiconductor Process Technology, and Packaging in line with India Semiconductor Mission. In addition, hands-on training in the cutting-edge area of chip design, semiconductor processing, and packaging are the key features.

Highlights of the course:

- Free Course
- Semiconductor Fab Lab Hands-on
- Expert Lecture and Demo of Semiconductor Packaging
- Industrial Visit: Semiconductor Fab and Packaging
- Government Certificate
- Job Counseling Sessions
- EDA Tool support under C2S programme

Eligibility:

- B.Tech: 6 semester onwards
- M.Sc: Second Year onwards
- Pursuing M.Tech/PhD in relevant areas
- Faculty members working in relevant area

Duration: 06 Weeks

Food and accommodation may be availed at institute hostels on a payment basis.

Limited no of seats: 25

Important Dates:

Last Date to Register: 01/05/2025
Date of Confirmation: 15/05/2025
Commencement of Course: 26/05/25

Register Here

Course Coordinators:

Dr. Deepak Joshi: d.joshi@eced.svnit.ac.in,
Dr. Vivek Garg: vivekg@eced.svnit.ac.in,
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Visit Department

IEEE Student Branch- SVNIT Surat
ChipIN
इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY सत्यमेव जयते
C-DAC
Chips to Startup Programme
IETE Student Branch- SVNIT Surat

Outline of the Program

S. No		Topic	Duration and Timings
1	**Semiconductor Process Technology and Packaging**	Semiconductor Process Technology 1	3 Weeks Monday to Friday Lectures: 3 Hours Lab: 3 Hours **Industry Visit (1-2 Days)**
		Semiconductor Process Technology 2 (Hands-On)	
		Semiconductor Packaging	
2	**VLSI Design**	Analog Circuit Design	3 Weeks Monday to Friday Lectures: 3 Hours Lab: 3 Hours
		Digital Circuit and System Design	
		SOC, ASIC Design and Verification	

Session

- Daily 6-hrs sessions
  9:30 am – 12:30 pm IST, 2:30 pm – 5:30 pm IST
- 3-hr lab sessions (2:30 pm – 5:30 pm IST)
- Short take-home quiz to reinforce the most important concepts taught in the day

Additional Benefits:

- Assignments to supplement lectures with hands-on experiments on EDA tools
- Sessions by Industry Leaders from top VLSI and EDA companies
- Summative quiz to assess learning
- Interaction with Industry leaders
- Semiconductor Fab Lab Hands-on
- Expert Lecture and Demo of Semiconductor Packaging
- Industrial Visit: Semiconductor Fab and Packaging