DEPARTMENT OF ELECTRONICS ENGINEERING
SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ICHCHHANATH, SURAT-395007 (GUJARAT)
website: www.svnit.ac.in

Ref No. Date: February 12, 2018

Recruitment of Project Staff on Purely Contract Basis

Applications are invited on prescribed format for the post of Lab engineer and Research/Project Associate on purely contract basis for one year (may be extended further) for MeitY, Government of India, New Delhi sponsored project entitled "Special Manpower Development Programme for Chips to System Design" at the institute. The application form and the details of all educational qualifications and relevant experience required for various positions are available on Institute website http://www.svnit.ac.in**.** Filled in application form must be submitted to **"Chief Investigator, SMDP - C2SD Project, Department of Electronics Engineering, S. V. National Institute of Technology, Surat, Gujarat – 395007"** on or before **2nd April, 2018** by either Registered Post or Speed Post. **All Candidates are also requested to fill up the details through online form :** https://goo.gl/forms/FPvuLrHJPor4R9ZH2. Also send duly filled and signed scanned application forms to Email-Id : c2sdsvnit@gmail.com

(Dr. A. D. Darji)
CI, SMDP - C2SD Project
SVNIT Surat.

Eligibility Criterion:

S. No	Post	Qualification	Experience	No. of. Posts / Duration	Consolidated Pay (Per Month)
1.	Lab Engineer	BE/B.Tech* in Electronics & Communication Engg./Electronics Engineering/Computer Engineering with 02 years experience OR M.E/M.Tech* in VLSI/Microelectronics.	CAD Tools Management (Licensing and Installation), Networking in Linux environment and Linux Server Management, Embedded Systems (Arduino, Cortex M3/M4), PCB Design	1 Post / 1 Year	Rs. 25,000 /-
2.	Research/ Project Associate	BE/B.Tech* in Electronics & Communication Engg./Electronics Engineering/Computer Engineering with 2 years experience OR M.E/M.Tech* in VLSI/Microelectronics.	VLSI/Microelectronics, Signal Processing, MATLAB, CAD Tools, FPGA Based System and Chip Design, (Schematic to GDS Flow –Analog Flow, RTL to GDS – Digital Flow)	1 Post / 1 Year	Rs. 17,000 /-

*Aggregate First Class/CGPA 6.5 in B.E/B.Tech/M.E/M.Tech

Note:

1. Candidate having minimum aggregate First Class/CGPA 6.5 in B.E/B.Tech/M.E/M.Tech can only apply.
2. The above positions are purely contractual for one year and can be extended to five year based on the performance evaluation every year.
3. The last date for receiving applications is **2nd April, 2018**.
4. Institute will not be responsible for any postal delay.
5. Applications received after last date will not be considered.
6. The list of shortlisted candidates will be displayed on the institute website within one week.
7. Interview/Test for the shortlisted candidates will be held on **13th April, 2018.** However, **final date/venue of Interview/Tests will be communicated in the intimation email.**
8. Candidates have to appear for interview with **Bio-Data, 2 Passport size Photos, Duly filled application form, Original Certificates and one set of self-attested photocopies**.
9. An applicant has to ensure the authenticity of information provided in support of experience claimed, other documents and photograph.
10. The qualification and experience may be relaxed at any point of time by the Institute for otherwise exceptional candidates.
11. **No TA/DA will be paid for appearing in the Interview**.
12. Candidate employed in institute/Industry must produce No-Objection Certificate (NOC) at the time of interview.
13. List of selected candidates will be displayed in the institute website within one week after interview.
14. Candidates who got selected may be allowed to enroll for Ph.D./M.Tech (By Research) program subject to the fulfillment of eligibility conditions of SVNIT, Surat.

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APPLICATION FORM

1.	Post applied for		Self Attested Photograph
2.	Name of the Candidate		
3.	Address of the Candidate		
4.	Father's Name		
5.	Date of Birth		
6.	Age as on last date of application	_____ Years_____ Months _____ Days	
7.	Contact No. (Mobile)		
8.	Email Id.		

9. Educational Qualification (Photocopy of certificate/degree must be attached)

Qualification	Subject/Discipline	Board/Institute/University	Year	% of marks/CGPA obtained (Aggregate)
10th or equivalent				
12th or equivalent				
Bachelor Degree				
Master Degree				
Ph.D.				
Master Degree Thesis Title				
Ph.D. Thesis Title				

8. Relevant Experience (Details of Employment in chronological order. Enclose a separate sheet duly authenticated under your signature if necessary)

Organization	Post Held	From	To	Pay Drawn	Nature of Duties

9.	**Total emoluments per month presently drawn.**	
10.	**Additional information if any, which you would like to mention in support of your suitability for the post, (attached separate sheet if necessary)**	

Declaration

I hereby declare that the information furnished above is true to the best of my knowledge and belief. If at any time it is found that I have concealed any information or have given any incorrect data, my candidature/appointment, may be cancelled/terminated, without any notice or compensation.

Place:
Date:

Signature of the Candidate