S.V. NATIONAL INSTITUTE OF TECHNOLOGY
SURAT, GUJRAT-395 007 (www.svnit.ac.in)
Electronics Engineering Department

Junior Research Fellow (JRF-01) position

Funded by

Board of Research in Nuclear Sciences (BRNS), Department of Atomic Energy (DAE), Government of India.

Department of Atomic Energy (DAE) Board of Research In Nuclear Sciences (BRNS) has sectioned research Project titled, "FPGA Based Adaptive Filter Algorithm Implementation for external noise cancellation" . As per the provisions of the project, it is proposed to employ a Project staff (JRF) for per following requirement on purely adhoc basis:

Name of the Post	Junior Research Fellow (JRF)- 1 post
Minimum Qualification	First class B.Tech. /B.E. (Electronics/Electronics and Communication Engineering)
Pay	25,000/- pm +HRA as per institute rules
Date &Time of Written Test and Interview	18/08/2017, 11:00 AM

Person having experience in HDL, FPGA based system Design, Embedded System, Instrumentation, and signal processing will be given preference. Candidate is expected to work on FPGA Based Adaptive Filter Algorithm Implementation for external noise cancellation. Work will be carried out in collaboration with Institute for Plasma Research (IPR), Gandhinagar, an autonomous institute under Department of Atomic Energy, India.

Interested candidates are requested to remain present with application on plain paper (with two PP size photographs), original certificates of educational qualifications, experience, certificate of proof of birth date and one set of photo copies (self-attested) of the documents at Office in Electronics Engineering Department on above mentioned date and time.

No TA/DA will be provided for attending the interview.

Anand

(Dr. Anand Darji)
Assistant Professor, ECED
Principal Investigator