REGISTRATION FORM

Name :_____

Qualification :_____

Designation :_____

Department :_____

Institute :_____

Contact Details :_____

Postal Address :_____

_____

Telephone :_____

E-mail :_____

Payment Details :_____

Payable at :_____

Whether accommodation needed.....Yes/No

Signature of Applicant

Official Seal & Signature of the competent authority

Date:_____

Place:_____

*Photo copies of registration forms may be used for multiple entries

Speaker

Engineers from CoreEL Technologies and faculties from SVNIT, Surat

Contact

Hemendra Kumar
hemend.nit@gmail.com
88498-37820 (M)

Sandeep Alatgi
Sandeep.a@coreel.com
78880-38146 (M)

NOTE

Only 30 participants will be selected on a first come first served basis. Intimation of selection will be only through email. Limited accommodation would be provided on payment and first-cum-first-serve basis.

Important Dates

Registration Starts: 18th November 2017
Registration Ends : 15th January 2018

Address of Correspondence

Prof. A. D. Darji/Prof. P. J. Engineer
Electronics Engineering Department,
Sardar Vallabhbhai National Institute of Technology Surat,
Po. Ichchhanath,
Gaurav Path,
Surat
Gujarat-395007

Hard copy of duly signed registration form with DD/Cheque should be sent to above mentioned address. Scanned copy of registration form and DD/Cheque can be sent to: sdsoc.svnit@gmail.com

Sardar Vallabhbhai
National Institute of Technology, Surat
in collaboration with
CoreEL Technologies(I) Pvt Ltd

is pleased to announce a
Two days workshop on
"System Design on Zynq using SDSoC"
January 18 - 19, 2018

Venue

Electronics Engineering Department,
Sardar Vallabhbhai National Institute of Technology Surat,
Gujarat-395007

Coordinators

Prof. A. D. Darji
Prof. P. J. Engineer

About workshop on "System Design on Zynq using SDSoC"

Pre-requisites

- Basic C programming experience
- Basic understanding of processor-based system

Course Overview

Day 1

- Zynq AP SoC architecture and Vivado IPI
- SDSoC tool overview
- **Lab 1: Getting started with SDSoC design flow**
  - Go through the process of using SDSoC to create a new project using available templates.
- Data motion networks
- **Lab 2: Pragmas and data motion networks**
  - Handling data movements between the soGware and hardware accelerators using various pragma and SDSoC API.
- Coding Considerations
- Profiling
- **Lab 3: Profiling application and create accelerators**
  - Profiling an application, analyzing the results, identifying function(s) for hardware implementation.

Day 2

- Estimation
- **Lab 4: Estimating accelerator performance**
  - Estimating the expected performance of an application when functions are targeted in hardware, without going through the entire build cycle.
- Debugging
- **Lab 5: Debugging software application**
  - Debugging software application targeting Standalone and Linux OS in SDSoC.
- Using C-callable libraries and multiple accelerators
- Improving performance with Vivado HLS
- **Lab 6: Fine-tuning with Vivado HLS**
  - Using various techniques and directives of Vivado HLS which can be used in SDSoC to improve design performance.

Skills Gained

After completing this workshop, you will be able to

- Understand the concept of "software-defined" systems on chip (SDSoC)
- Understand the capabilities and limitations of the SDSoC development environment
- Get hands-on experience creating application-specific systems on chip from C/C++ programs using the SDSoC
- Gain practical understanding of the SDSoC design flow
  - How the SDSoC compiler maps programs to HW/SW systems
    - Structure of generated hardware systems
    - Structure of the generated software
  - How to control the compilation and generation process
    - Modifying program source
    - Using #pragmas

Registration

The registration is open to faculty members from engineering colleges, industry professionals, PG students, research associates and research scholars. The registration fee for participation is as follows:

Academicians	Rs. 1200/-
Students	Rs. 1000/-
Industry Professionals	Rs. 2500/-

Registration fee includes workshop kit, tea/snacks and lunch.

The fees may be paid by DD/Cheque in favor of "Director, SVNIT - CCE" payable at Surat.

About SVNIT

The Sardar Vallabhbhai National Institute of Technology was established in 1961 as one of the RECs. University Grants Commission, has declared the Sardar Vallabhbhai Regional College of Engineering & Technology (SVREC), Surat to Sardar Vallabhbhai National Institute of Technology (SVNIT), Surat with status of "Deemed University" with effect from 4th December 2002. The Institute has been granted the status of 'Institute of National Importance' w.e.f. Aug. 15, 2007. At present, the Institute is offering Six UG Programmes, Eighteen PG Programmes and Three M.Sc. Five Years Integrated Programme including doctoral programme in all above branches.

About Electronics Engineering Department

In the year 1983-84, the UG program in Electronics Engineering was introduced. Electronics Engineering Department is conducting two M. Tech. programs with specialization in "Communication Systems" and "VLSI & Embedded Systems". VLSI Lab in Electronics Engineering Department contains the well-established research facilities in the field of VLSI design both in analog and digital domain. Well known EDA tools from reputed vendors such as Synopsys, Mentor Graphics, Cadence, Xilinx and Altium are available for front-end and back-end VLSI design flow as well as device simulation.

About CoreEL

CoreEL Technologies is a Customer Application Specific Product & Solutions (CASPS) company offering innovative solutions from its diverse portfolio that includes Intellectual Property (IP) cores, System Design, Manufacturing, Sustenance, Next-gen products, and OEM solutions, in the form of EDA tools,CAE tools, COTS products and Technology training. CoreEL's strength lies in its ability to blend deep domain knowledge with the right ingredients across its portfolio of offerings. It is a leading developer of advanced electronic system level products and solutions to three primary markets – Aerospace & Defence, Digital Media Broadcast, and Universities & Institutions of higher learning.